

Sitronix

zerocap  芯零携 

ST77916

**360RGB x 390 262K Color with Display Ram
Single-Chip TFT Controller/Driver**

Datasheet

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1 GENERAL DESCRIPTION

The ST77916 is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. The 540-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The ST77916 is capable of connecting directly to an external microprocessor, and provides 8-bits parallel interface, 6-bit RGB Interface, MIPI interface, 3/4-line serial peripheral interface (3/4 SPI), and Quad serial peripheral interface (QSPI).

Display data can be stored in the on-chip display data RAM of 360x390x18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption.

In addition, because of the integrated power supply circuit necessary to drive liquid crystal; it is possible to make a display system with fewest components.

2 FEATURES

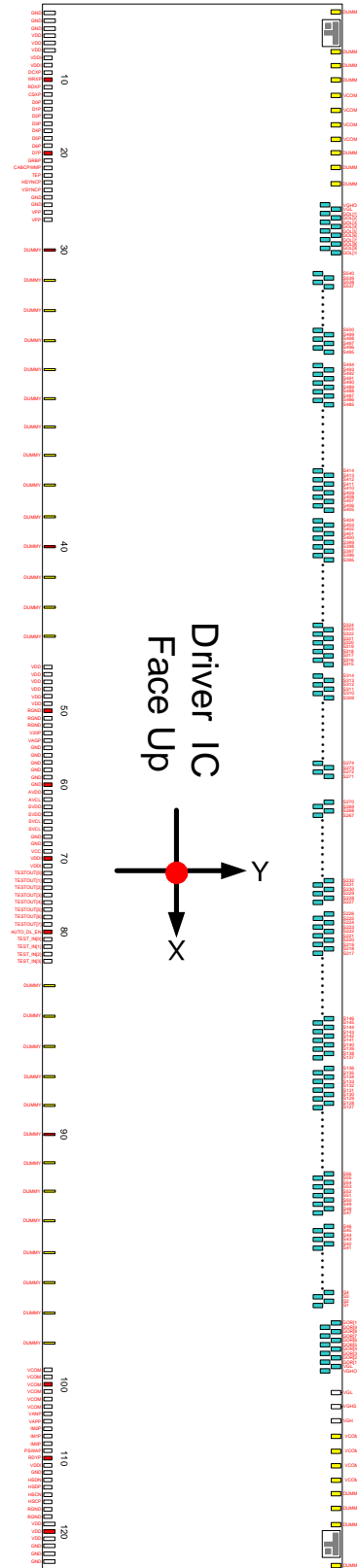
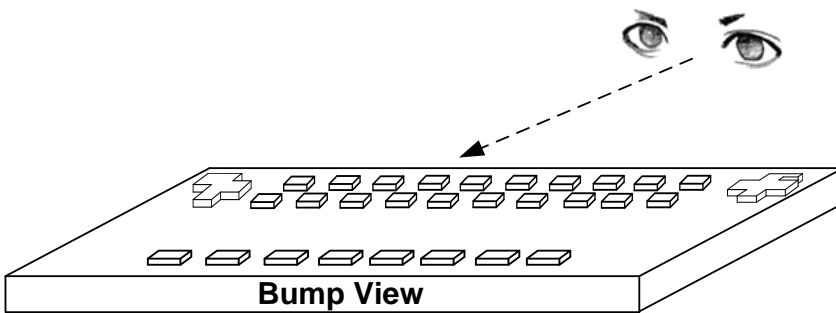
- Single chip TFT-LCD Controller/Driver with On-chip Display RAM
- Display Resolution: 360*RGB (H) *390(V)
- LCD Driver Output Circuits
 - Source Outputs: 540 RGB Channels
 - Support gate control signals to gate driver in the panel
- Display Colors (Color Mode)
 - Full Color: 262K, RGB=(666) max., Idle Mode Off
 - Color Reduce: 8-color, RGB=(111), Idle Mode On
- Programmable Pixel Color Format (Color Depth) for Various Display Data Input Format
 - 16-bit/pixel: RGB=(565) 65K color
 - 18-bit/pixel: RGB=(666) 262K color
- Interface
 - Parallel 8080-series MCU Interface (8-bit)
 - 6-bit RGB Interface (VSYNCX, HSYNCX, DOTCLK, ENABLE, DB[5:0])
 - Serial Peripheral Interface (SPI Interface) and 2 data lane SPI
 - Quad Serial Peripheral Interface (QSPI Interface)
 - MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 data lane pairs)
- Display Features
 - 1 Gamma (64 gray levels)
 - Brightness Control Block
 - CDC Function
- On Chip Build-In Circuits
 - DC/DC Converter
 - Non-Volatile (NV) Memory
 - Adjustable VCOM Generation
 - Timing Controller
 - Internal VPP for NV Memory
- Build-In NV Memory for LCD Initial Register Setting
 - OTP to store ID1~ID3
 - OTP to store VCOM/VCC/VREGP/VREGN calibration
 - OTP to store CDC and Factory Default Value (Module ID, Module Version, and etc.)
 - OTP to store panel timing, analog power setting, and etc.
- Driving Algorithm
 - 1/2/4-dot Inversion
 - Column Inversion
- Wide Supply Voltage Range

- I/O Voltage (VDDI to GND): 1.65V ~ 3.3V ($VDDI \leq VDD$)
- Voltage for Analog Circuit (VDD to GND): 2.65V ~ 3.3V
- On-Chip Power System
 - VCOM level: GND
 - Gamma(+) voltage range: 3.65V~6.2V
 - Gamma(-) voltage range: -4.2V~-1.875V
 - VGH voltage range: 11.0V~15.5V
 - VGL voltage range: -8.4V~-11.7V
 - Adjustable voltage range for feed through compensation: 0.1V~2.2V
- Power saving modes
 - Sleep in mode
 - Deep Sleep in mode
 - Deep Standby mode
 - Low frame mode 1~50Hz
- Others
 - Zero-Cap (Gate <390)
 - GIP + Dual-Gate driving
 - Single-Gate: pixel number must be a multiple of 4 (* If need Horizontal Scroll, the Pixel number must be a multiple of 12)
 - Dual-Gate: pixel number must be a multiple of 8 (* If need Horizontal Scroll, the Pixel number must be a multiple of 24)
 - The Source number must be a multiple of 12 and no fewer than 276
(* If need Horizontal Scroll, the Source number must be a multiple of 36 and no fewer than 288)
- Optimized layout for COG Assembly
- Operate temperature range: -30°C to +85 °C
- Lower Power Consumption

3 PAD ARRANGEMENT

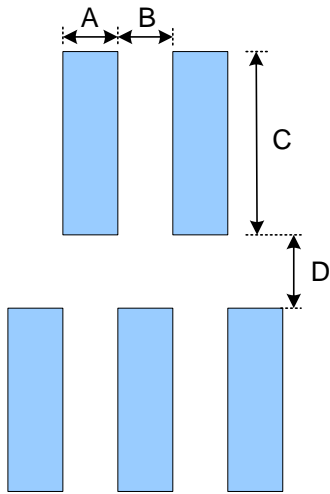
3.1 Output Bump Dimension

Au bump height	9um
Au bump size	13μm x 80μm : Dummy 、 VCOM 、 VCOML 、 VGH 、 VGHS 、 VGL GIP : VGHOR 、 VGHOL 、 VGL 、 GO1~GO10 Source : S1~S540
	30μm x 100μm : Pad 1 to Pad 6 、 Pad 119 to Pad 124
	30μm x 75μm : Pad 7 to Pad 29 、 Pad 44 to Pad 84 、 Pad 98 to Pad 118
	15μm x 75μm : Pad 30 to Pad 43 、 Pad 85 to Pad 97



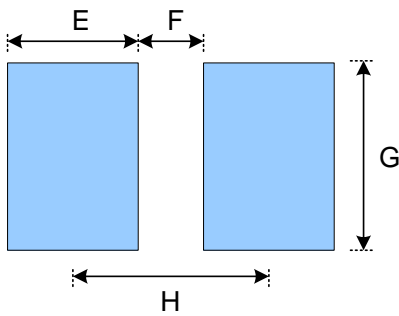
3.2 Bump Dimension

●Output Pads

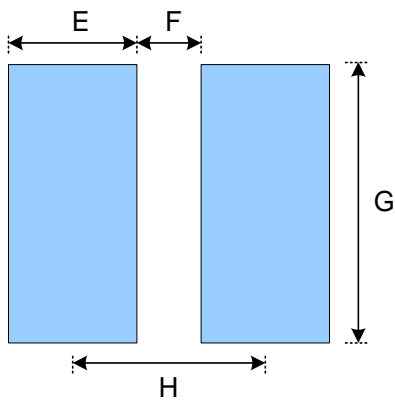


Symbol	Item	Size
A	Bump Width	13 um
B	Bump Gap 1 (Horizontal)	15 um
C	Bump Height	80 um
D	Bump Gap 2 (Vertical)	20 um

●Input Pads



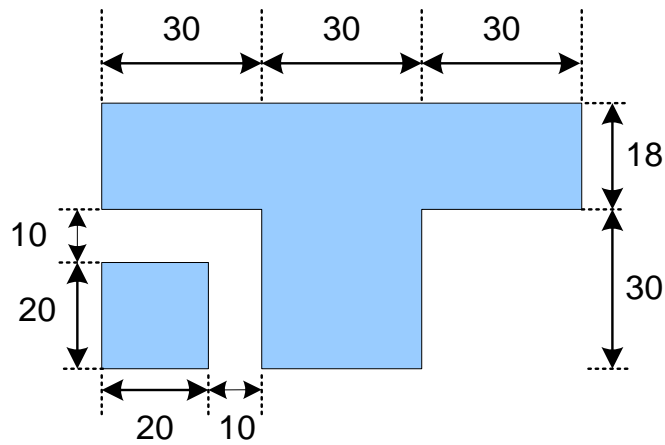
Symbol	Item	Size
E	Bump Width	30 um
F	Bump Gap	15 um
G	Bump Height	75 um
H	Bump Pitch	45 or 49 um



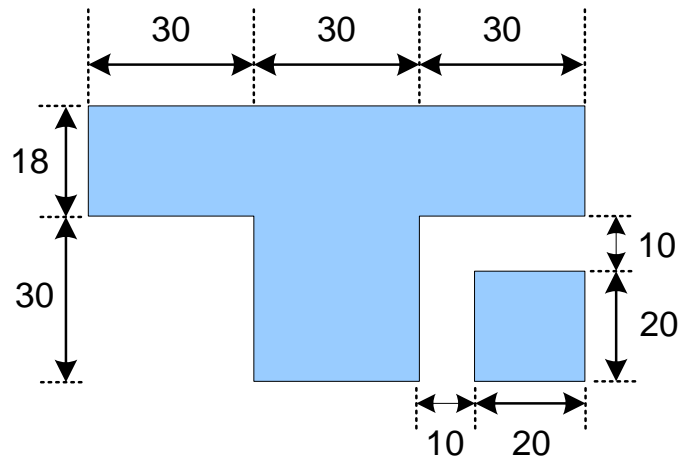
Symbol	Item	Size
E	Bump Width	30 um
F	Bump Gap	15 um
G	Bump Height	100 um
H	Bump Pitch	45 um

3.3 Alignment Mark Dimension

●Alignment Mark Left: L(X,Y)=(-5504.25, 375.1)



●Alignment Mark Right: R(X,Y)= (5504.25, 375.1)



3.4 Chip Information

Chip size	11326 um x 826 um
Chip thickness	250um
Pad Location	Pad center
Coordinate Origin	Chip center

Note: The chip size is not include the scribe line.

4 PAD ARRANGEMENT

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	GND	-5617.5	-355	34	DUMMY	-3148.35	-367.5
2	GND	-5572.5	-355	35	DUMMY	-2912.85	-367.5
3	GND	-5527.5	-355	36	DUMMY	-2677.35	-367.5
4	VDD	-5482.5	-355	37	DUMMY	-2441.85	-367.5
5	VDD	-5437.5	-355	38	DUMMY	-2206.35	-367.5
6	VDD	-5392.5	-355	39	DUMMY	-1970.85	-367.5
7	VDDI	-5347.5	-367.5	40	DUMMY	-1735.35	-367.5
8	VDDI	-5302.5	-367.5	41	DUMMY	-1499.85	-367.5
9	DCXP	-5257.5	-367.5	42	DUMMY	-1264.35	-367.5
10	WRXP	-5212.5	-367.5	43	DUMMY	-1028.6	-367.5
11	RDXP	-5167.5	-367.5	44	VDD	-785.5	-367.5
12	CSXP	-5122.5	-367.5	45	VDD	-740.5	-367.5
13	D0P	-5077.5	-367.5	46	VDD	-695.5	-367.5
14	D1P	-5028.5	-367.5	47	VDD	-650.5	-367.5
15	D2P	-4979.5	-367.5	48	VDD	-605.5	-367.5
16	D3P	-4930.5	-367.5	49	VDD	-560.5	-367.5
17	D4P	-4881.5	-367.5	50	RGND	-515.5	-367.5
18	D5P	-4832.5	-367.5	51	RGND	-470.5	-367.5
19	D6P	-4783.5	-367.5	52	RGND	-425.5	-367.5
20	D7P	-4738.5	-367.5	53	V20P	-380.5	-367.5
21	GRBP	-4693.5	-367.5	54	VAGP	-335.5	-367.5
22	CABCPWMP	-4648.5	-367.5	55	GND	-290.5	-367.5
23	TEP	-4603.5	-367.5	56	GND	-245.5	-367.5
24	HSYNCP	-4558.5	-367.5	57	GND	-200.5	-367.5
25	VSYNCP	-4513.5	-367.5	58	GND	-155.5	-367.5
26	GND	-4468.5	-367.5	59	GND	-110.5	-367.5
27	GND	-4423.5	-367.5	60	GND	-65.5	-367.5
28	VPP	-4378.5	-367.5	61	AVDD	-20.5	-367.5
29	VPP	-4333.5	-367.5	62	AVCL	24.5	-367.5
30	DUMMY	-4090.35	-367.5	63	SVDD	69.5	-367.5
31	DUMMY	-3854.85	-367.5	64	SVDD	114.5	-367.5
32	DUMMY	-3619.35	-367.5	65	SVCL	159.5	-367.5
33	DUMMY	-3383.85	-367.5	66	SVCL	204.5	-367.5

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
67	GND	249.5	-367.5	101	VCOM	4582.5	-367.5
68	GND	294.5	-367.5	102	VCOM	4627.5	-367.5
69	VCC	339.5	-367.5	103	VCOM	4672.5	-367.5
70	VDDI	384.5	-367.5	104	VANP	4717.5	-367.5
71	VDDI	429.5	-367.5	105	VAPP	4762.5	-367.5
72	TESTOUTP[0]	474.5	-367.5	106	IM2P	4807.5	-367.5
73	TESTOUTP[1]	519.5	-367.5	107	IM1P	4852.5	-367.5
74	TESTOUTP[2]	564.5	-367.5	108	IM0P	4897.5	-367.5
75	TESTOUTP[3]	609.5	-367.5	109	PSWAP	4942.5	-367.5
76	TESTOUTP[4]	654.5	-367.5	110	RDYP	4987.5	-367.5
77	TESTOUTP[5]	699.5	-367.5	111	VDDI	5032.5	-367.5
78	TESTOUTP[6]	744.5	-367.5	112	GND	5077.5	-367.5
79	TESTOUTP[7]	789.5	-367.5	113	DN	5122.5	-367.5
80	AUTO_DL_ENP	834.5	-367.5	114	DP	5167.5	-367.5
81	TEST_INP[0]	879.5	-367.5	115	CN	5212.5	-367.5
82	TEST_INP[1]	924.5	-367.5	116	CP	5257.5	-367.5
83	TEST_INP[2]	969.5	-367.5	117	RGND	5302.5	-367.5
84	TEST_INP[3]	1014.5	-367.5	118	RGND	5347.5	-367.5
85	DUMMY	1267	-367.5	119	VDD	5392.5	-355
86	DUMMY	1511	-367.5	120	VDD	5437.5	-355
87	DUMMY	1755	-367.5	121	VDD	5482.5	-355
88	DUMMY	1999	-367.5	122	GND	5527.5	-355
89	DUMMY	2243	-367.5	123	GND	5572.5	-355
90	DUMMY	2487	-367.5	124	GND	5617.5	-355
91	DUMMY	2731	-367.5	125	DUMMY	5626	365
92	DUMMY	2975	-367.5	126	DUMMY	5415	365
93	DUMMY	3219	-367.5	127	DUMMY	5325	365
94	DUMMY	3463	-367.5	128	DUMMY	5235	365
95	DUMMY	3707	-367.5	129	VCOM	5145	365
96	DUMMY	3951	-367.5	130	VCOM	5055	365
97	DUMMY	4195	-367.5	131	VCOM	4965	365
98	VCOM	4447.5	-367.5	132	VCOM	4875	365
99	VCOM	4492.5	-367.5	133	VGH	4785	365
100	VCOM	4537.5	-367.5	134	VGHS	4695	365

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
135	VGL	4605	365	169	SO[22]	3893.5	303.3
136	VGHOR	4455.5	265	170	SO[23]	3879.5	203.3
137	VGL	4441.5	365	171	SO[24]	3865.5	303.3
138	GOR[1]	4427.5	265	172	SO[25]	3851.5	203.3
139	GOR[2]	4413.5	365	173	SO[26]	3837.5	303.3
140	GOR[3]	4399.5	265	174	SO[27]	3823.5	203.3
141	GOR[4]	4385.5	365	175	SO[28]	3809.5	303.3
142	GOR[5]	4371.5	265	176	SO[29]	3795.5	203.3
143	GOR[6]	4357.5	365	177	SO[30]	3781.5	303.3
144	GOR[7]	4343.5	265	178	SO[31]	3767.5	203.3
145	GOR[8]	4329.5	365	179	SO[32]	3753.5	303.3
146	GOR[9]	4315.5	265	180	SO[33]	3739.5	203.3
147	GOR[10]	4301.5	365	181	SO[34]	3725.5	303.3
148	SO[1]	4187.5	203.3	182	SO[35]	3711.5	203.3
149	SO[2]	4173.5	303.3	183	SO[36]	3697.5	303.3
150	SO[3]	4159.5	203.3	184	SO[37]	3683.5	203.3
151	SO[4]	4145.5	303.3	185	SO[38]	3669.5	303.3
152	SO[5]	4131.5	203.3	186	SO[39]	3655.5	203.3
153	SO[6]	4117.5	303.3	187	SO[40]	3641.5	303.3
154	SO[7]	4103.5	203.3	188	SO[41]	3627.5	203.3
155	SO[8]	4089.5	303.3	189	SO[42]	3613.5	303.3
156	SO[9]	4075.5	203.3	190	SO[43]	3599.5	203.3
157	SO[10]	4061.5	303.3	191	SO[44]	3585.5	303.3
158	SO[11]	4047.5	203.3	192	SO[45]	3571.5	203.3
159	SO[12]	4033.5	303.3	193	SO[46]	3557.5	303.3
160	SO[13]	4019.5	203.3	194	SO[47]	3435	203.3
161	SO[14]	4005.5	303.3	195	SO[48]	3421	303.3
162	SO[15]	3991.5	203.3	196	SO[49]	3407	203.3
163	SO[16]	3977.5	303.3	197	SO[50]	3393	303.3
164	SO[17]	3963.5	203.3	198	SO[51]	3379	203.3
165	SO[18]	3949.5	303.3	199	SO[52]	3365	303.3
166	SO[19]	3935.5	203.3	200	SO[53]	3351	203.3
167	SO[20]	3921.5	303.3	201	SO[54]	3337	303.3
168	SO[21]	3907.5	203.3	202	SO[55]	3323	203.3

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
203	SO[56]	3309	303.3	237	SO[90]	2833	303.3
204	SO[57]	3295	203.3	238	SO[91]	2819	203.3
205	SO[58]	3281	303.3	239	SO[92]	2805	303.3
206	SO[59]	3267	203.3	240	SO[93]	2791	203.3
207	SO[60]	3253	303.3	241	SO[94]	2777	303.3
208	SO[61]	3239	203.3	242	SO[95]	2763	203.3
209	SO[62]	3225	303.3	243	SO[96]	2749	303.3
210	SO[63]	3211	203.3	244	SO[97]	2735	203.3
211	SO[64]	3197	303.3	245	SO[98]	2721	303.3
212	SO[65]	3183	203.3	246	SO[99]	2707	203.3
213	SO[66]	3169	303.3	247	SO[100]	2693	303.3
214	SO[67]	3155	203.3	248	SO[101]	2679	203.3
215	SO[68]	3141	303.3	249	SO[102]	2665	303.3
216	SO[69]	3127	203.3	250	SO[103]	2651	203.3
217	SO[70]	3113	303.3	251	SO[104]	2637	303.3
218	SO[71]	3099	203.3	252	SO[105]	2623	203.3
219	SO[72]	3085	303.3	253	SO[106]	2609	303.3
220	SO[73]	3071	203.3	254	SO[107]	2595	203.3
221	SO[74]	3057	303.3	255	SO[108]	2581	303.3
222	SO[75]	3043	203.3	256	SO[109]	2567	203.3
223	SO[76]	3029	303.3	257	SO[110]	2553	303.3
224	SO[77]	3015	203.3	258	SO[111]	2539	203.3
225	SO[78]	3001	303.3	259	SO[112]	2525	303.3
226	SO[79]	2987	203.3	260	SO[113]	2511	203.3
227	SO[80]	2973	303.3	261	SO[114]	2497	303.3
228	SO[81]	2959	203.3	262	SO[115]	2483	203.3
229	SO[82]	2945	303.3	263	SO[116]	2469	303.3
230	SO[83]	2931	203.3	264	SO[117]	2455	203.3
231	SO[84]	2917	303.3	265	SO[118]	2441	303.3
232	SO[85]	2903	203.3	266	SO[119]	2427	203.3
233	SO[86]	2889	303.3	267	SO[120]	2413	303.3
234	SO[87]	2875	203.3	268	SO[121]	2399	203.3
235	SO[88]	2861	303.3	269	SO[122]	2385	303.3
236	SO[89]	2847	203.3	270	SO[123]	2371	203.3

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
271	SO[124]	2357	303.3	305	SO[158]	1772.5	303.3
272	SO[125]	2343	203.3	306	SO[159]	1758.5	203.3
273	SO[126]	2329	303.3	307	SO[160]	1744.5	303.3
274	SO[127]	2315	203.3	308	SO[161]	1730.5	203.3
275	SO[128]	2301	303.3	309	SO[162]	1716.5	303.3
276	SO[129]	2287	203.3	310	SO[163]	1702.5	203.3
277	SO[130]	2273	303.3	311	SO[164]	1688.5	303.3
278	SO[131]	2259	203.3	312	SO[165]	1674.5	203.3
279	SO[132]	2245	303.3	313	SO[166]	1660.5	303.3
280	SO[133]	2231	203.3	314	SO[167]	1646.5	203.3
281	SO[134]	2217	303.3	315	SO[168]	1632.5	303.3
282	SO[135]	2203	203.3	316	SO[169]	1618.5	203.3
283	SO[136]	2189	303.3	317	SO[170]	1604.5	303.3
284	SO[137]	2066.5	203.3	318	SO[171]	1590.5	203.3
285	SO[138]	2052.5	303.3	319	SO[172]	1576.5	303.3
286	SO[139]	2038.5	203.3	320	SO[173]	1562.5	203.3
287	SO[140]	2024.5	303.3	321	SO[174]	1548.5	303.3
288	SO[141]	2010.5	203.3	322	SO[175]	1534.5	203.3
289	SO[142]	1996.5	303.3	323	SO[176]	1520.5	303.3
290	SO[143]	1982.5	203.3	324	SO[177]	1506.5	203.3
291	SO[144]	1968.5	303.3	325	SO[178]	1492.5	303.3
292	SO[145]	1954.5	203.3	326	SO[179]	1478.5	203.3
293	SO[146]	1940.5	303.3	327	SO[180]	1464.5	303.3
294	SO[147]	1926.5	203.3	328	SO[181]	1450.5	203.3
295	SO[148]	1912.5	303.3	329	SO[182]	1436.5	303.3
296	SO[149]	1898.5	203.3	330	SO[183]	1422.5	203.3
297	SO[150]	1884.5	303.3	331	SO[184]	1408.5	303.3
298	SO[151]	1870.5	203.3	332	SO[185]	1394.5	203.3
299	SO[152]	1856.5	303.3	333	SO[186]	1380.5	303.3
300	SO[153]	1842.5	203.3	334	SO[187]	1366.5	203.3
301	SO[154]	1828.5	303.3	335	SO[188]	1352.5	303.3
302	SO[155]	1814.5	203.3	336	SO[189]	1338.5	203.3
303	SO[156]	1800.5	303.3	337	SO[190]	1324.5	303.3
304	SO[157]	1786.5	203.3	338	SO[191]	1310.5	203.3

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
339	SO[192]	1296.5	303.3	373	SO[226]	820.5	303.3
340	SO[193]	1282.5	203.3	374	SO[227]	669.5	203.3
341	SO[194]	1268.5	303.3	375	SO[228]	655.5	303.3
342	SO[195]	1254.5	203.3	376	SO[229]	641.5	203.3
343	SO[196]	1240.5	303.3	377	SO[230]	627.5	303.3
344	SO[197]	1226.5	203.3	378	SO[231]	613.5	203.3
345	SO[198]	1212.5	303.3	379	SO[232]	599.5	303.3
346	SO[199]	1198.5	203.3	380	SO[233]	585.5	203.3
347	SO[200]	1184.5	303.3	381	SO[234]	571.5	303.3
348	SO[201]	1170.5	203.3	382	SO[235]	557.5	203.3
349	SO[202]	1156.5	303.3	383	SO[236]	543.5	303.3
350	SO[203]	1142.5	203.3	384	SO[237]	529.5	203.3
351	SO[204]	1128.5	303.3	385	SO[238]	515.5	303.3
352	SO[205]	1114.5	203.3	386	SO[239]	501.5	203.3
353	SO[206]	1100.5	303.3	387	SO[240]	487.5	303.3
354	SO[207]	1086.5	203.3	388	SO[241]	473.5	203.3
355	SO[208]	1072.5	303.3	389	SO[242]	459.5	303.3
356	SO[209]	1058.5	203.3	390	SO[243]	445.5	203.3
357	SO[210]	1044.5	303.3	391	SO[244]	431.5	303.3
358	SO[211]	1030.5	203.3	392	SO[245]	417.5	203.3
359	SO[212]	1016.5	303.3	393	SO[246]	403.5	303.3
360	SO[213]	1002.5	203.3	394	SO[247]	389.5	203.3
361	SO[214]	988.5	303.3	395	SO[248]	375.5	303.3
362	SO[215]	974.5	203.3	396	SO[249]	361.5	203.3
363	SO[216]	960.5	303.3	397	SO[250]	347.5	303.3
364	SO[217]	946.5	203.3	398	SO[251]	333.5	203.3
365	SO[218]	932.5	303.3	399	SO[252]	319.5	303.3
366	SO[219]	918.5	203.3	400	SO[253]	305.5	203.3
367	SO[220]	904.5	303.3	401	SO[254]	291.5	303.3
368	SO[221]	890.5	203.3	402	SO[255]	277.5	203.3
369	SO[222]	876.5	303.3	403	SO[256]	263.5	303.3
370	SO[223]	862.5	203.3	404	SO[257]	249.5	203.3
371	SO[224]	848.5	303.3	405	SO[258]	235.5	303.3
372	SO[225]	834.5	203.3	406	SO[259]	221.5	203.3

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
407	SO[260]	207.5	303.3	441	SO[294]	-389.5	203.3
408	SO[261]	193.5	203.3	442	SO[295]	-403.5	303.3
409	SO[262]	179.5	303.3	443	SO[296]	-417.5	203.3
410	SO[263]	165.5	203.3	444	SO[297]	-431.5	303.3
411	SO[264]	151.5	303.3	445	SO[298]	-445.5	203.3
412	SO[265]	137.5	203.3	446	SO[299]	-459.5	303.3
413	SO[266]	123.5	303.3	447	SO[300]	-473.5	203.3
414	SO[267]	109.5	203.3	448	SO[301]	-487.5	303.3
415	SO[268]	95.5	303.3	449	SO[302]	-501.5	203.3
416	SO[269]	81.5	203.3	450	SO[303]	-515.5	303.3
417	SO[270]	67.5	303.3	451	SO[304]	-529.5	203.3
418	SO[271]	-67.5	303.3	452	SO[305]	-543.5	303.3
419	SO[272]	-81.5	203.3	453	SO[306]	-557.5	203.3
420	SO[273]	-95.5	303.3	454	SO[307]	-571.5	303.3
421	SO[274]	-109.5	203.3	455	SO[308]	-585.5	203.3
422	SO[275]	-123.5	303.3	456	SO[309]	-599.5	303.3
423	SO[276]	-137.5	203.3	457	SO[310]	-613.5	203.3
424	SO[277]	-151.5	303.3	458	SO[311]	-627.5	303.3
425	SO[278]	-165.5	203.3	459	SO[312]	-641.5	203.3
426	SO[279]	-179.5	303.3	460	SO[313]	-655.5	303.3
427	SO[280]	-193.5	203.3	461	SO[314]	-669.5	203.3
428	SO[281]	-207.5	303.3	462	SO[315]	-820.5	303.3
429	SO[282]	-221.5	203.3	463	SO[316]	-834.5	203.3
430	SO[283]	-235.5	303.3	464	SO[317]	-848.5	303.3
431	SO[284]	-249.5	203.3	465	SO[318]	-862.5	203.3
432	SO[285]	-263.5	303.3	466	SO[319]	-876.5	303.3
433	SO[286]	-277.5	203.3	467	SO[320]	-890.5	203.3
434	SO[287]	-291.5	303.3	468	SO[321]	-904.5	303.3
435	SO[288]	-305.5	203.3	469	SO[322]	-918.5	203.3
436	SO[289]	-319.5	303.3	470	SO[323]	-932.5	303.3
437	SO[290]	-333.5	203.3	471	SO[324]	-946.5	203.3
438	SO[291]	-347.5	303.3	472	SO[325]	-960.5	303.3
439	SO[292]	-361.5	203.3	473	SO[326]	-974.5	203.3
440	SO[293]	-375.5	303.3	474	SO[327]	-988.5	303.3

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
475	SO[328]	-1002.5	203.3	509	SO[362]	-1478.5	203.3
476	SO[329]	-1016.5	303.3	510	SO[363]	-1492.5	303.3
477	SO[330]	-1030.5	203.3	511	SO[364]	-1506.5	203.3
478	SO[331]	-1044.5	303.3	512	SO[365]	-1520.5	303.3
479	SO[332]	-1058.5	203.3	513	SO[366]	-1534.5	203.3
480	SO[333]	-1072.5	303.3	514	SO[367]	-1548.5	303.3
481	SO[334]	-1086.5	203.3	515	SO[368]	-1562.5	203.3
482	SO[335]	-1100.5	303.3	516	SO[369]	-1576.5	303.3
483	SO[336]	-1114.5	203.3	517	SO[370]	-1590.5	203.3
484	SO[337]	-1128.5	303.3	518	SO[371]	-1604.5	303.3
485	SO[338]	-1142.5	203.3	519	SO[372]	-1618.5	203.3
486	SO[339]	-1156.5	303.3	520	SO[373]	-1632.5	303.3
487	SO[340]	-1170.5	203.3	521	SO[374]	-1646.5	203.3
488	SO[341]	-1184.5	303.3	522	SO[375]	-1660.5	303.3
489	SO[342]	-1198.5	203.3	523	SO[376]	-1674.5	203.3
490	SO[343]	-1212.5	303.3	524	SO[377]	-1688.5	303.3
491	SO[344]	-1226.5	203.3	525	SO[378]	-1702.5	203.3
492	SO[345]	-1240.5	303.3	526	SO[379]	-1716.5	303.3
493	SO[346]	-1254.5	203.3	527	SO[380]	-1730.5	203.3
494	SO[347]	-1268.5	303.3	528	SO[381]	-1744.5	303.3
495	SO[348]	-1282.5	203.3	529	SO[382]	-1758.5	203.3
496	SO[349]	-1296.5	303.3	530	SO[383]	-1772.5	303.3
497	SO[350]	-1310.5	203.3	531	SO[384]	-1786.5	203.3
498	SO[351]	-1324.5	303.3	532	SO[385]	-1800.5	303.3
499	SO[352]	-1338.5	203.3	533	SO[386]	-1814.5	203.3
500	SO[353]	-1352.5	303.3	534	SO[387]	-1828.5	303.3
501	SO[354]	-1366.5	203.3	535	SO[388]	-1842.5	203.3
502	SO[355]	-1380.5	303.3	536	SO[389]	-1856.5	303.3
503	SO[356]	-1394.5	203.3	537	SO[390]	-1870.5	203.3
504	SO[357]	-1408.5	303.3	538	SO[391]	-1884.5	303.3
505	SO[358]	-1422.5	203.3	539	SO[392]	-1898.5	203.3
506	SO[359]	-1436.5	303.3	540	SO[393]	-1912.5	303.3
507	SO[360]	-1450.5	203.3	541	SO[394]	-1926.5	203.3
508	SO[361]	-1464.5	303.3	542	SO[395]	-1940.5	303.3

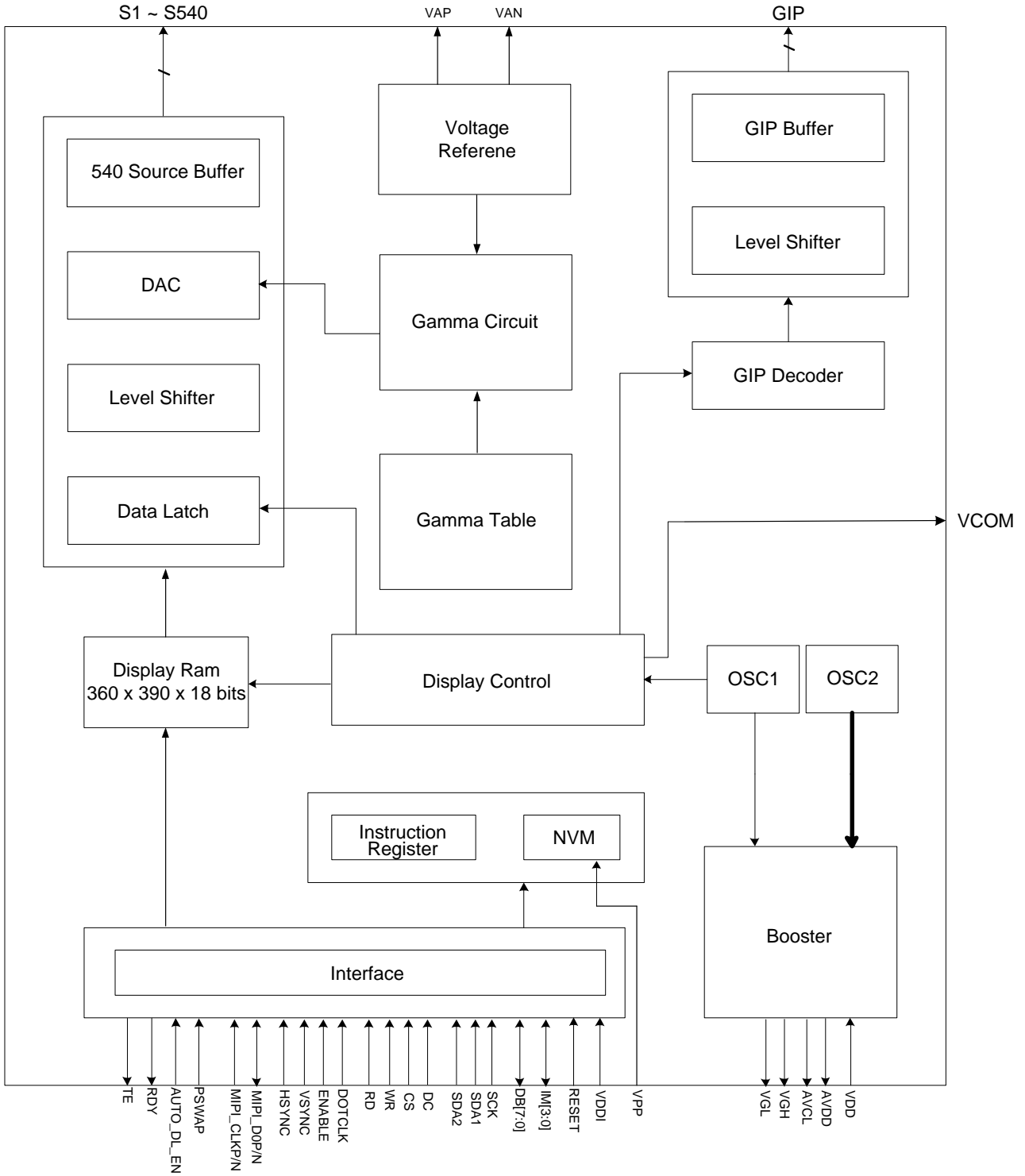
PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
543	SO[396]	-1954.5	203.3	577	SO[430]	-2539	203.3
544	SO[397]	-1968.5	303.3	578	SO[431]	-2553	303.3
545	SO[398]	-1982.5	203.3	579	SO[432]	-2567	203.3
546	SO[399]	-1996.5	303.3	580	SO[433]	-2581	303.3
547	SO[400]	-2010.5	203.3	581	SO[434]	-2595	203.3
548	SO[401]	-2024.5	303.3	582	SO[435]	-2609	303.3
549	SO[402]	-2038.5	203.3	583	SO[436]	-2623	203.3
550	SO[403]	-2052.5	303.3	584	SO[437]	-2637	303.3
551	SO[404]	-2066.5	203.3	585	SO[438]	-2651	203.3
552	SO[405]	-2189	303.3	586	SO[439]	-2665	303.3
553	SO[406]	-2203	203.3	587	SO[440]	-2679	203.3
554	SO[407]	-2217	303.3	588	SO[441]	-2693	303.3
555	SO[408]	-2231	203.3	589	SO[442]	-2707	203.3
556	SO[409]	-2245	303.3	590	SO[443]	-2721	303.3
557	SO[410]	-2259	203.3	591	SO[444]	-2735	203.3
558	SO[411]	-2273	303.3	592	SO[445]	-2749	303.3
559	SO[412]	-2287	203.3	593	SO[446]	-2763	203.3
560	SO[413]	-2301	303.3	594	SO[447]	-2777	303.3
561	SO[414]	-2315	203.3	595	SO[448]	-2791	203.3
562	SO[415]	-2329	303.3	596	SO[449]	-2805	303.3
563	SO[416]	-2343	203.3	597	SO[450]	-2819	203.3
564	SO[417]	-2357	303.3	598	SO[451]	-2833	303.3
565	SO[418]	-2371	203.3	599	SO[452]	-2847	203.3
566	SO[419]	-2385	303.3	600	SO[453]	-2861	303.3
567	SO[420]	-2399	203.3	601	SO[454]	-2875	203.3
568	SO[421]	-2413	303.3	602	SO[455]	-2889	303.3
569	SO[422]	-2427	203.3	603	SO[456]	-2903	203.3
570	SO[423]	-2441	303.3	604	SO[457]	-2917	303.3
571	SO[424]	-2455	203.3	605	SO[458]	-2931	203.3
572	SO[425]	-2469	303.3	606	SO[459]	-2945	303.3
573	SO[426]	-2483	203.3	607	SO[460]	-2959	203.3
574	SO[427]	-2497	303.3	608	SO[461]	-2973	303.3
575	SO[428]	-2511	203.3	609	SO[462]	-2987	203.3
576	SO[429]	-2525	303.3	610	SO[463]	-3001	303.3

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
611	SO[464]	-3015	203.3	645	SO[498]	-3599.5	203.3
612	SO[465]	-3029	303.3	646	SO[499]	-3613.5	303.3
613	SO[466]	-3043	203.3	647	SO[500]	-3627.5	203.3
614	SO[467]	-3057	303.3	648	SO[501]	-3641.5	303.3
615	SO[468]	-3071	203.3	649	SO[502]	-3655.5	203.3
616	SO[469]	-3085	303.3	650	SO[503]	-3669.5	303.3
617	SO[470]	-3099	203.3	651	SO[504]	-3683.5	203.3
618	SO[471]	-3113	303.3	652	SO[505]	-3697.5	303.3
619	SO[472]	-3127	203.3	653	SO[506]	-3711.5	203.3
620	SO[473]	-3141	303.3	654	SO[507]	-3725.5	303.3
621	SO[474]	-3155	203.3	655	SO[508]	-3739.5	203.3
622	SO[475]	-3169	303.3	656	SO[509]	-3753.5	303.3
623	SO[476]	-3183	203.3	657	SO[510]	-3767.5	203.3
624	SO[477]	-3197	303.3	658	SO[511]	-3781.5	303.3
625	SO[478]	-3211	203.3	659	SO[512]	-3795.5	203.3
626	SO[479]	-3225	303.3	660	SO[513]	-3809.5	303.3
627	SO[480]	-3239	203.3	661	SO[514]	-3823.5	203.3
628	SO[481]	-3253	303.3	662	SO[515]	-3837.5	303.3
629	SO[482]	-3267	203.3	663	SO[516]	-3851.5	203.3
630	SO[483]	-3281	303.3	664	SO[517]	-3865.5	303.3
631	SO[484]	-3295	203.3	665	SO[518]	-3879.5	203.3
632	SO[485]	-3309	303.3	666	SO[519]	-3893.5	303.3
633	SO[486]	-3323	203.3	667	SO[520]	-3907.5	203.3
634	SO[487]	-3337	303.3	668	SO[521]	-3921.5	303.3
635	SO[488]	-3351	203.3	669	SO[522]	-3935.5	203.3
636	SO[489]	-3365	303.3	670	SO[523]	-3949.5	303.3
637	SO[490]	-3379	203.3	671	SO[524]	-3963.5	203.3
638	SO[491]	-3393	303.3	672	SO[525]	-3977.5	303.3
639	SO[492]	-3407	203.3	673	SO[526]	-3991.5	203.3
640	SO[493]	-3421	303.3	674	SO[527]	-4005.5	303.3
641	SO[494]	-3435	203.3	675	SO[528]	-4019.5	203.3
642	SO[495]	-3557.5	303.3	676	SO[529]	-4033.5	303.3
643	SO[496]	-3571.5	203.3	677	SO[530]	-4047.5	203.3
644	SO[497]	-3585.5	303.3	678	SO[531]	-4061.5	303.3

PAD No.	PIN Name	X	Y
679	SO[532]	-4075.5	203.3
680	SO[533]	-4089.5	303.3
681	SO[534]	-4103.5	203.3
682	SO[535]	-4117.5	303.3
683	SO[536]	-4131.5	203.3
684	SO[537]	-4145.5	303.3
685	SO[538]	-4159.5	203.3
686	SO[539]	-4173.5	303.3
687	SO[540]	-4187.5	203.3
688	GOL[10]	-4301.5	365
689	GOL[9]	-4315.5	265
690	GOL[8]	-4329.5	365
691	GOL[7]	-4343.5	265
692	GOL[6]	-4357.5	365
693	GOL[5]	-4371.5	265
694	GOL[4]	-4385.5	365
695	GOL[3]	-4399.5	265
696	GOL[2]	-4413.5	365
697	GOL[1]	-4427.5	265
698	VGL	-4441.5	365
699	VGHOL	-4455.5	265
700	DUMMY	-4605	365
701	DUMMY	-4695	365
702	DUMMY	-4785	365
703	VCOML	-4875	365
704	VCOML	-4965	365
705	VCOML	-5055	365
706	VCOML	-5145	365
707	DUMMY	-5235	365
708	DUMMY	-5325	365
709	DUMMY	-5415	365
710	DUMMY	-5626	365

Note: The Pad Location is not include the Temperature Compensation (TC).

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1 Power Supply Pins

Name	I/O	Description	Connect Pin
VDD	I	- Power Supply for Analog, Digital System and Booster Circuit.	VDD
VDDI	I	- Power Supply for I/O System. - VDDI must be lower than or equal to VDD.	VDDI
GND	I	- System Ground for Analog System, Digital System, I/O System and Booster Circuit.	GND
RGND	I	- System Ground for Reference Circuit.	GND
VPP	I	- Power Supply for Internal NVM. - When programming NVM, It needs external power supply voltage (7.5V). - The current of Ivpp must be more than 10mA. - If not used, Leaves these pins open.	External Power

6.2 Interface Logic Pins

Name	I/O	Description	Connect Pin																																													
IM2P IM1P IM0P	I	<p>-The System interface mode select.</p> <table border="1"> <thead> <tr> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>MPU Interface Mode</th> <th>Data pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>3-line 9bit serial I/F</td> <td>SDA: in/out</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>MIPI I/F</td> <td>SDA: in/out \ DP/DN</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>2 data lane serial I/F</td> <td>SDA1: in/out \ SDA2: in</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>QSPI I/F</td> <td>SDA[3:0]: in/out</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>RGB_3-line 9bit serial I/F</td> <td>SDA: in/out \ DB[5:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>RGB_4-line 8bit serial I/F</td> <td>SDA: in/out \ DB[5:0]</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>4-line 8bit serial I/F</td> <td>SDA: in/out</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>80-8bit parallel I/F</td> <td>DB[7:0]</td> </tr> </tbody> </table>	IM2	IM1	IM0	MPU Interface Mode	Data pin	0	0	0	3-line 9bit serial I/F	SDA: in/out	0	0	1	MIPI I/F	SDA: in/out \ DP/DN	0	1	0	2 data lane serial I/F	SDA1: in/out \ SDA2: in	0	1	1	QSPI I/F	SDA[3:0]: in/out	1	0	0	RGB_3-line 9bit serial I/F	SDA: in/out \ DB[5:0]	1	0	1	RGB_4-line 8bit serial I/F	SDA: in/out \ DB[5:0]	1	1	0	4-line 8bit serial I/F	SDA: in/out	1	1	1	80-8bit parallel I/F	DB[7:0]	GND/VDDI
IM2	IM1	IM0	MPU Interface Mode	Data pin																																												
0	0	0	3-line 9bit serial I/F	SDA: in/out																																												
0	0	1	MIPI I/F	SDA: in/out \ DP/DN																																												
0	1	0	2 data lane serial I/F	SDA1: in/out \ SDA2: in																																												
0	1	1	QSPI I/F	SDA[3:0]: in/out																																												
1	0	0	RGB_3-line 9bit serial I/F	SDA: in/out \ DB[5:0]																																												
1	0	1	RGB_4-line 8bit serial I/F	SDA: in/out \ DB[5:0]																																												
1	1	0	4-line 8bit serial I/F	SDA: in/out																																												
1	1	1	80-8bit parallel I/F	DB[7:0]																																												
GRBP	I	<p>-This signal will reset the device and it must be applied to properly initialize the chip. -Signal is active low.</p>	MCU																																													
D[7:0]P	I/O	<p>-D[7:0]P are used as MCU parallel interface data bus. 8-bit parallel I/F: D[7:0]P are used. -D[7:0]P are used as SPI interface data bus. 8-bit serial I/F: D0P is used. (SDA) 9-bit serial I/F: D0P is used. (SDA)</p>	MCU																																													

Name	I/O	Description	Connect Pin																									
		2 data lane serial I/F: D[1:0]P are used. (SDA1、SDA2) -D[7:0]P are used as QSPI interface data bus. Single: D0P is used. (SDA0) Dual: D[1:0]P are used. (SDA0、SDA1) Quad: D[3:0]P are used. (SDA0、SDA1、SDA2、SDA3) - D[7:0]P are used as RGB interface data bus. 6-bit RGB I/F: D[7:2]P are used. ; D1P is used. (DE) -If not used, please fix this pin at VDDI or GND.																										
TEP	O	-Tearing effect signal is used to synchronize MCU to frame memory writing. -If not used, please let this pin open.	MCU																									
CSXP	I	-Chip select pin. Low enable. High disable	MCU																									
DCXP	I	-Display data/command selection pin in parallel interface. DCX='1': display data or parameter. DCX='0': command data. -Display data/command selection pin in 4-line serial interface. (A0) DCX='1': display data or parameter. DCX='0': command data. -If not used, please fix this pin at VDDI or GND.	MCU																									
WRXP	I	-Write enable in MCU parallel interface. - Dot clock signal in RGB interface. (DOTCLK) -If not used, please fix this pin at VDDI or GND.	MCU																									
RDXP	I	-Read enable in MCU parallel interface. - Clock in SPI interface. (SCL) -If not used, please fix this pin at VDDI or GND.	MCU																									
HSYNCP	I	-Horizontal (Line) synchronizing input signal in RGB interface. -If not used, please fix to the VDDI or GND.	MCU																									
VSYNCP	I	-Vertical (Frame) synchronizing input signal in RGB interface. -If not used, please fix to the VDDI or GND.	MCU																									
PSWAP	I	-Differential clock polarity swap in MIPI-DSI interface. <table border="1" style="margin: 10px auto;"> <thead> <tr> <th rowspan="2">PSWAP</th> <th rowspan="2">IM2</th> <th rowspan="2">IM1</th> <th rowspan="2">IM0</th> <th colspan="4">MIPI I/F</th> </tr> <tr> <th>HSCP</th> <th>HSCN</th> <th>HSDP</th> <th>HSDN</th> </tr> </thead> <tbody> <tr> <td>0</td> <td rowspan="2">0</td> <td rowspan="2">0</td> <td rowspan="2">1</td> <td>HSCP</td> <td>HSCN</td> <td>HSDP</td> <td>HSDN</td> </tr> <tr> <td>1</td> <td>HSCN</td> <td>HSCP</td> <td>HSDN</td> <td>HSDP</td> </tr> </tbody> </table>	PSWAP	IM2	IM1	IM0	MIPI I/F				HSCP	HSCN	HSDP	HSDN	0	0	0	1	HSCP	HSCN	HSDP	HSDN	1	HSCN	HSCP	HSDN	HSDP	GND/VDDI
PSWAP	IM2	IM1					IM0	MIPI I/F																				
			HSCP	HSCN	HSDP	HSDN																						
0	0	0	1	HSCP	HSCN	HSDP	HSDN																					
1				HSCN	HSCP	HSDN	HSDP																					
CP	I	-MIPI-DSI clock lane positive-end input pin.	MCU																									

Name	I/O	Description	Connect Pin						
		-If not used, please fix this pin at GND.							
CN	I	-MIPI-DSI clock lane negative-end input pin. -If not used, please fix this pin at GND.	MCU						
DP	I/O	-MIPI-DSI data lane positive-end input pin. -If not used, please fix this pin at GND.	MCU						
DN	I/O	-MIPI-DSI data lane negative-end input pin. -If not used, please fix this pin at GND.	MCU						
AUTO_DL_ENP	I	-OTP trim function control pin. -When normal display, this pin should be set to "H" and the value in the OTP will be downloaded automatically. <table border="1" data-bbox="501 689 1166 846"> <thead> <tr> <th>AUTO_DL_ENP</th> <th>Function Description</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>Disable auto-refresh function</td> </tr> <tr> <td>H</td> <td>Enable auto-refresh function(Default)</td> </tr> </tbody> </table>	AUTO_DL_ENP	Function Description	L	Disable auto-refresh function	H	Enable auto-refresh function(Default)	GND/VDDI
AUTO_DL_ENP	Function Description								
L	Disable auto-refresh function								
H	Enable auto-refresh function(Default)								
RDYP	O	-Compressed processing busy flag is used to notice Host that compressed processing has completed. -If not used, please let this pin open.	MCU						

6.3 Driver Output Pins

Name	I/O	Description	Connect pin
S[540:1]	O	-Source output voltage signals applied to liquid crystal.	LCD
GOR[10:1] GOL[10:1]	O	-Gate control signals and the swing voltage level is VGH to VGL.	LCD
VGHOR	O	-Power output (Positive) pin for gate driver.	LCD
VGHOL	O	-Power output (Positive) pin for gate driver.	LCD
VCOM	O	-A power supply for the TFT-LCD common electrode.	GND
VCOML	O	-A power supply for the TFT-LCD common electrode.	GND
VGH	O	-Power output pin for gate driver. -If not used, please let this pin open.	LCD
VGL	O	-Power output (Negative) pin for gate driver. -If not used, please let this pin open.	LCD
VGHS	O	-Power output pin for gate driver. (pump) -If not used, please let this pin open.	LCD
CABCPWM	O	-PWM output signal to driving LED. -If not used, please let this pin open.	-

Note: Use Power Pad(VGL · VGHOR · VGHOL) instead of assigning GIP, if VGL and VGH are needed in Panel.

6.4 Test and Other Pins

Name	I/O	Description	Connect pin
Dummy	-	-These pins are dummy. -Leave the pin open.	OPEN
SVEE	O	-Used for monitoring. -Leave the pin open.	OPEN
SVDD	O	-Used for monitoring. -Leave the pin open.	OPEN
VCC	O	-Used for monitoring. -Leave the pin open.	OPEN
AVDD	O	-Power Pad for analog Circuit. -Leave the pin open.	OPEN
AVEE	O	-Power Pad for analog Circuit. -Leave the pin open.	OPEN
VAPP	O	-A power output of grayscale voltage. -Leave the pin open.	OPEN
VANP	O	-A power output (negative) of gray scale voltage. -Leave the pin open.	OPEN
VAG	O	-This pin is for testing. -Leave the pin open.	OPEN
V20P	O	-Used for monitoring. -Leave the pin open.	OPEN
TESTOUTPUT[7:0]	O	-This pin is for testing -Leave the pin open.	OPEN
TEST_INP[3:0]	I	-This pin is for testing -Leave the pin open.	OPEN

7 DRIVER ELECTRICAL CHARACTERISTICS

7.1 Absolute Operation Range

Item	Symbol	Range	Unit
Supply Voltage (Analog)	VDD	- 0.3 ~ +4.6	V
Supply Voltage (I/O)	VDDI	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VCC	-0.3 ~ +2	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	0.5 ~ VDDI + 0.5	V
Logic Output Voltage Range	VO	0.5 ~ VDDI + 0.5	V
Operating Temperature Range	TOPR	-30 ~ +85	°C
Storage Temperature Range	TSTG	-40 ~ +125	°C

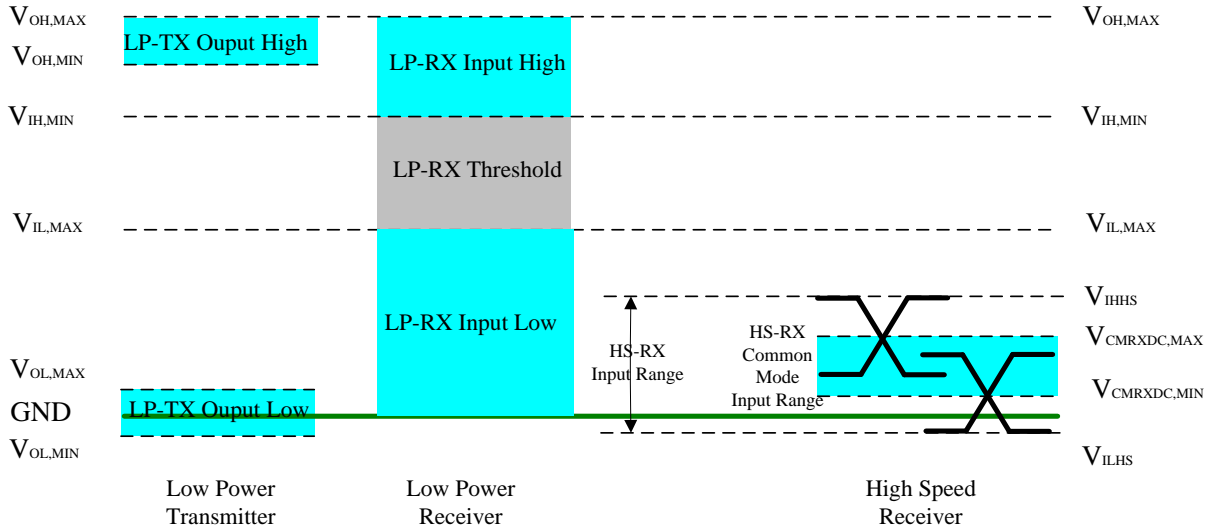
Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 DC Characteristics

7.2.1 DC characteristics for MIPI DSI

●MIPI Signaling Voltage Levels



●MIPI DC characteristics

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	V_{LPH}	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Logic 0 input threshold	V_{IL}	0	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	1350	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V

7.2.2 DC characteristics for Panel Driving

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD	Operating voltage	2.65	2.8	3.3	V	-
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	-
Gate Driver High Voltage	VGH	-	11.0	-	15.5	V	-
Gate Driver Low Voltage	VGL	-	-11.7	-	-8.4	V	-
Gate Driver Supply Voltage	-	VGH-VGL	-	-	27.2	V	-
Input / Output							
Logic-High Input Voltage	VIH	-	0.7VDDI	-	VDDI	V	Note 1
Logic-Low Input Voltage	VIL	-	GND	-	0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI	-	VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	GND	-	0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI	-	-	1	uA	Note 1
Logic-Low Input Current	IIL	VIN = GND	-1	-	-	uA	Note 1
Input Leakage Current	IIL	IOH = -1.0mA	-0.1	-	+0.1	uA	Note 1
VCOM Voltage							
VCOM Voltage	VCOM	-	-	GND	-	V	-
Source Driver							
Gamma Reference Voltage(Positive)	VAP	-	3.65	-	6.2	V	-
Gamma Reference Voltage(Negative)	VAN	-	-4.2	-	-1.875	-	-
Source Output Settling Time	Tr	Below with 99% precision	-	-	20	us	Note 2
Output Offset Voltage	VOFFSET	-	-	-	35	mV	Note 3

Basic DC Characteristics

Notes:

1. TA= -30 to 85°C.
2. The max. value is between measured point of source output and gamma setting value.
3. The Max. Value is between measured point of source output and gamma setting value.

7.3 Power Consumption

T_a=25°C, Frame rate = 60Hz, Registers setting are IC default setting.

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDD1 (mA)	IDD (mA)	IDD1 (mA)	IDD (mA)
Normal Mode	Note	0.001	8	0.005	10
Sleep-in Mode	Note	0.001	0.030	0.005	0.150
Deep Standby Mode	Note	0.001	0.001	0.005	0.005

Notes:

1. Color Picture.
2. The Current Consumption is DC characteristics of ST77916.
3. Condition: VDD1=1.8V, VDD=2.8V.

7.4 AC Characteristics

7.4.1 8080 Series MCU Parallel Interface Characteristics: 8-bit Bus

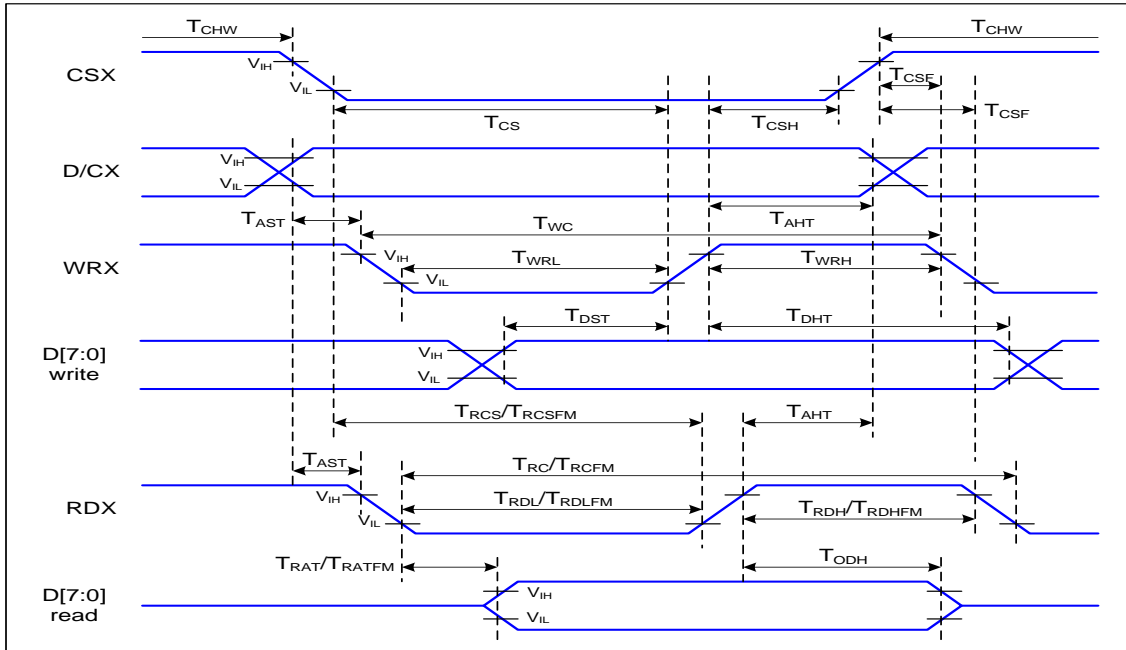


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

$V_{DDI}=1.65$ to $3.3V$, $V_{DD}=2.65$ to $3.3V$, $GND=RGND=0V$, $T_a=25^{\circ}C$

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	-
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	-
	T_{RCS}	Chip select setup time (Read ID)	45		ns	-
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	-
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	-
	T_{CSH}	Chip select hold time	10		ns	-
WRX	T_{WC}	Write cycle	30		ns	-
	T_{WRH}	Control pulse "H" duration	14		ns	-
	T_{WRL}	Control pulse "L" duration	14		ns	-
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	

	$T_{RD LFM}$	Control pulse "L" duration (FM)		355		ns	
D[7:0]	T_{DST}	Data setup time		10		ns	For CL=30pF
	T_{DHT}	Data hold time		10		ns	
	T_{RAT}	Read access time (ID)			40	ns	
	T_{RATFM}	Read access time (FM)			340	ns	
	T_{ODH}	Output disable time		20	80	ns	

Table 1 8080 Parallel Interface Characteristics

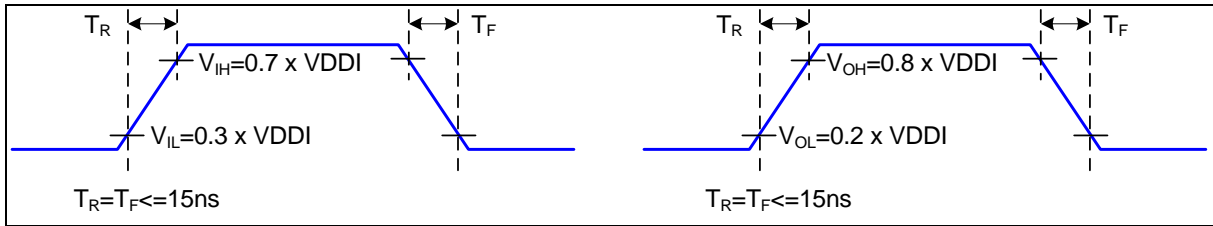


Figure 2 Rising and Falling Timing for I/O Signal

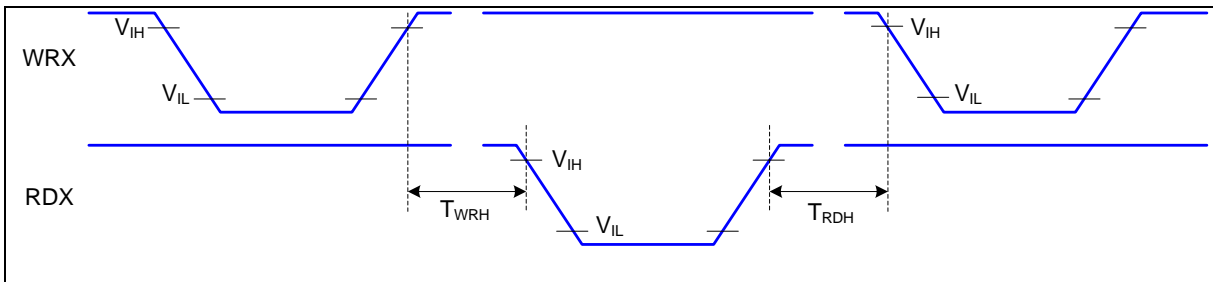


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (T_r , T_f) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.2 Serial Interface Characteristics (3-line serial):

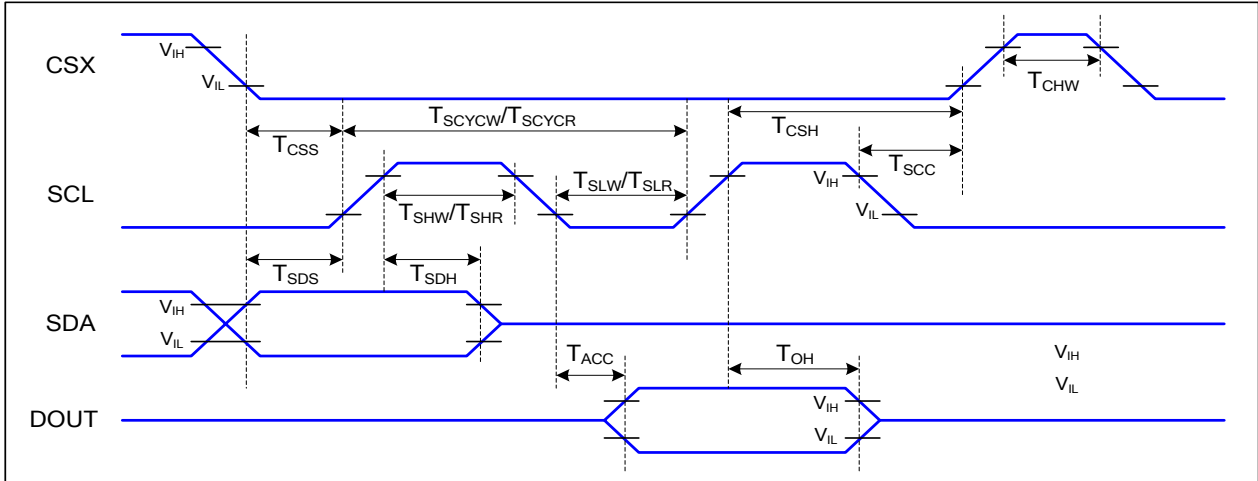


Figure 4 3-line serial Interface Timing Characteristics

V_{DDI}=1.65 to 3.3V, V_{DD}=2.65 to 3.3V, G_{ND}=RG_{ND}=0V, T_a=25°C

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T _{CSS}	Chip select setup time (write)	15		ns	
	T _{CSS}	Chip select setup time (read)	60		ns	
	T _{CSS}	Chip select hold time (write)	15		ns	
	T _{SCC}	Chip select hold time (read)	65		ns	
	T _{CHW}	Chip select "H" pulse width	40		ns	
SCL	T _{SCYCW}	Serial clock cycle (Write)	16		ns	
	T _{SHW}	SCL "H" pulse width (Write)	7		ns	
	T _{SLW}	SCL "L" pulse width (Write)	7		ns	
	T _{SCYCR}	Serial clock cycle (Read)	150		ns	
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	
	T _{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T _{SDS}	Data setup time	10		ns	
	T _{SDH}	Data hold time	10		ns	
DOUT	T _{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T _{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 2 3-line serial Interface Characteristics

Note : The rising time and falling time (T_r, T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of V_{DDI} for Input signals.

7.4.3 Serial Interface Characteristics (4-line serial):

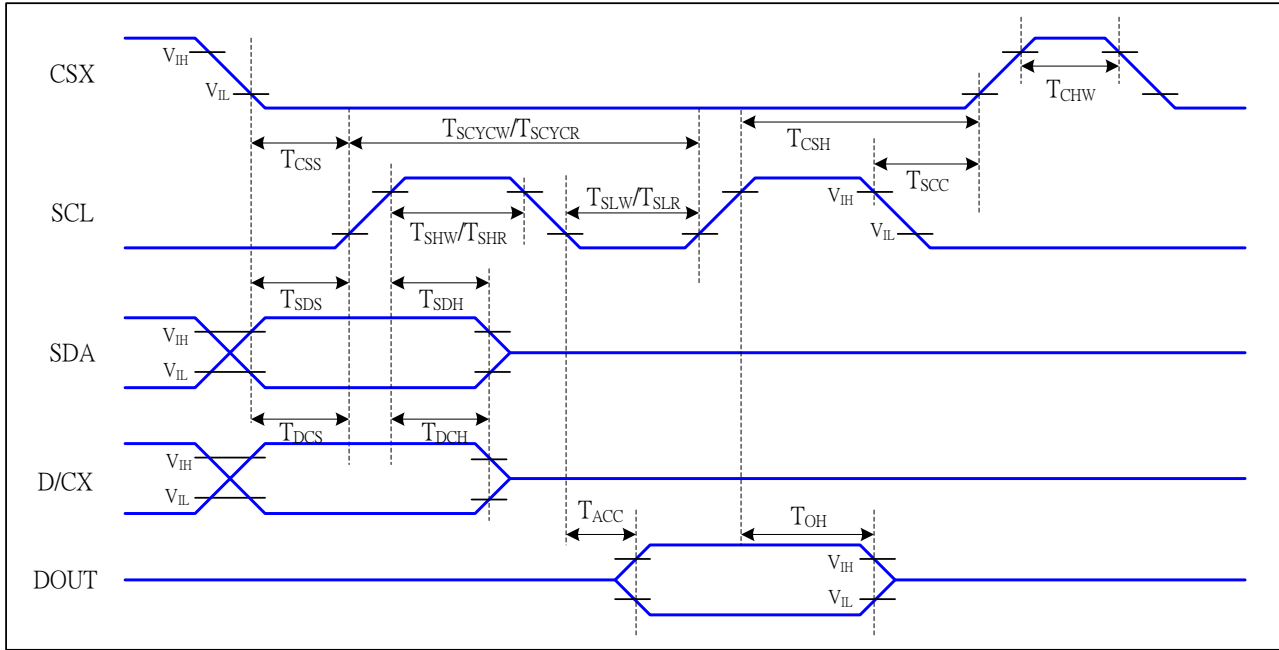


Figure 5 4-line serial Interface Timing Characteristics

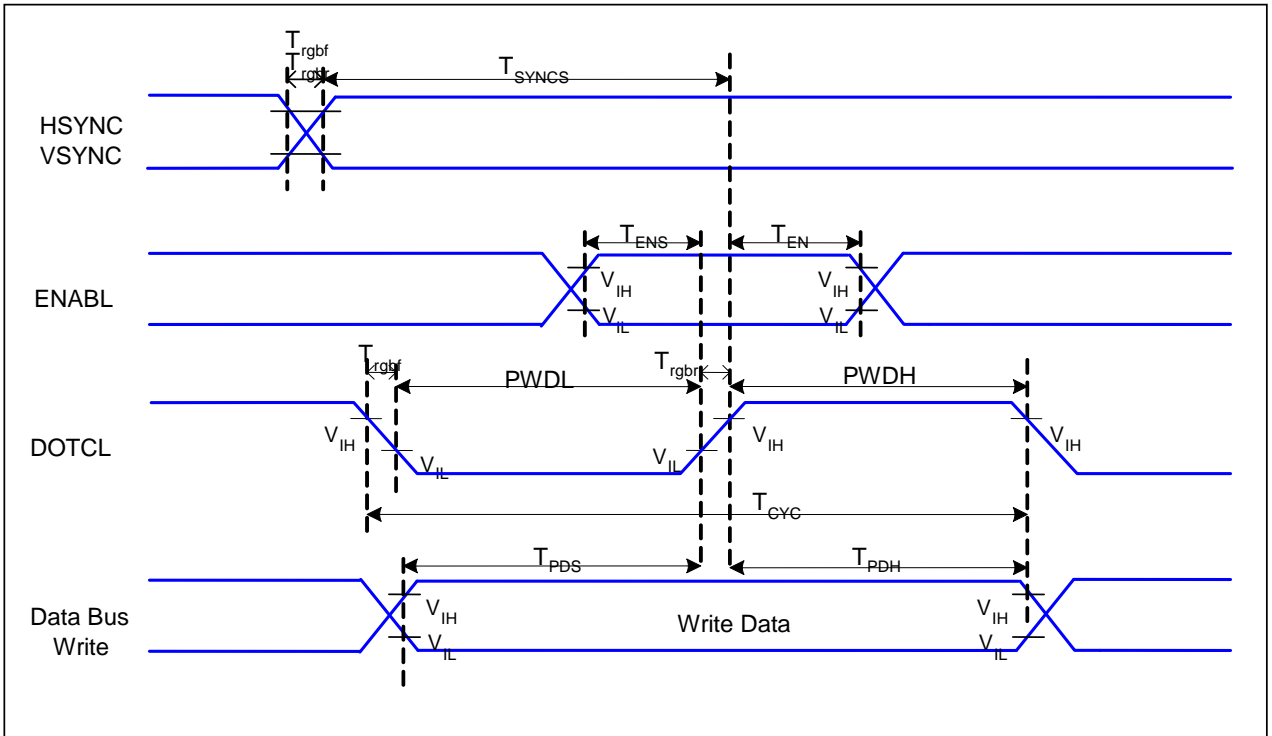
V_{DDI}=1.65 to 3.3V, V_{DD}=2.65 to 3.3V, G_{ND}=R_{GN}D=0V, T_a=25°C

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T _{CSS}	Chip select setup time (write)	15		ns	
	T _{CSH}	Chip select hold time (write)	15		ns	
	T _{CSS}	Chip select setup time (read)	60		ns	
	T _{SCC}	Chip select hold time (read)	65		ns	
	T _{CHW}	Chip select "H" pulse width	40		ns	
SCL	T _{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T _{SHW}	SCL "H" pulse width (Write)	7		ns	
	T _{SLW}	SCL "L" pulse width (Write)	7		ns	
	T _{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	
	T _{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T _{DCS}	D/CX setup time	7		ns	
	T _{DCH}	D/CX hold time	7		ns	
SDA (DIN)	T _{SDS}	Data setup time	10		ns	
	T _{SDH}	Data hold time	10		ns	
DOUT	T _{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T _{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 3 4-line serial Interface Characteristics

Note : The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.4.4 RGB Interface Characteristics:



$V_{\text{DDI}}=1.65$ to 3.3V , $V_{\text{DD}}=2.65$ to 3.3V , $\text{GND}=\text{RGND}=0\text{V}$, $T_{\text{a}}=25^{\circ}\text{C}$

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCNS}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	35	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	10	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

Table 4 6 Bits RGB Interface Timing Characteristics

7.4.5 QSPI Interface Characteristics:

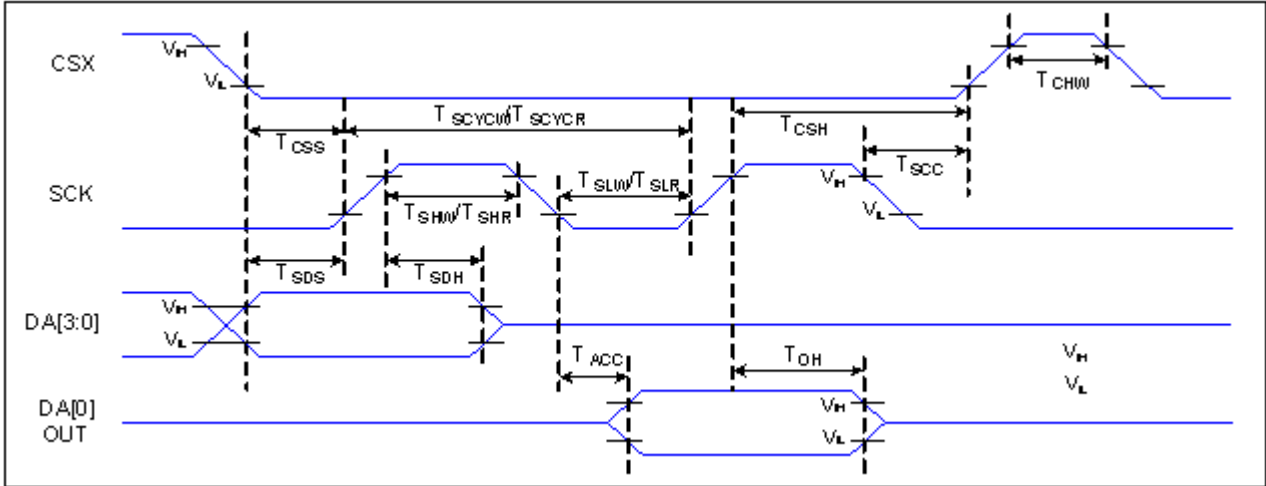


Figure 7 QSPI Interface Timing Characteristics

V_{DDI}=1.65 to 3.3V, V_{DD}=2.65 to 3.3V, G_{ND}=R_{GND}=0V, T_a=25°C

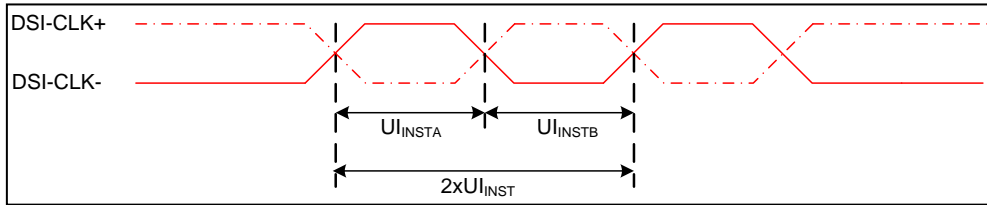
Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T _{CSS}	Chip select setup time (write)	15		ns	
	T _{CSH}	Chip select hold time (write)	15		ns	
	T _{CSS}	Chip select setup time (read)	60		ns	
	T _{SCC}	Chip select hold time (read)	65		ns	
	T _{CHW}	Chip select "H" pulse width	40		ns	
			200		ns	Note 1
SCL	T _{SCYCW}	Serial clock cycle (Write)	16		ns	
	T _{SHW}	SCL "H" pulse width (Write)	7		ns	
	T _{SLW}	SCL "L" pulse width (Write)	7		ns	
	T _{SCYCR}	Serial clock cycle (Read)	150		ns	
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	
	T _{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T _{SDS}	Data setup time	7		ns	
	T _{SDH}	Data hold time	7		ns	
DOUT	T _{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T _{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 QSPI Interface Characteristics

Note : The rising time and falling time (T_r, T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of V_{DDI} for Input signals.

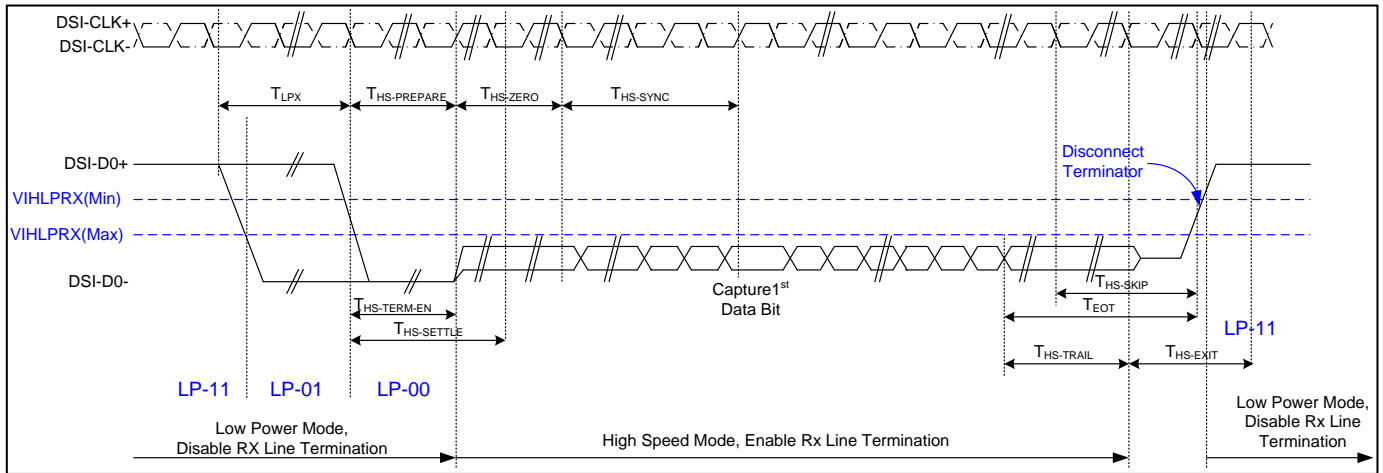
7.4.6 MIPI Interface Characteristics

High Speed Mode – Clock Channel Timing



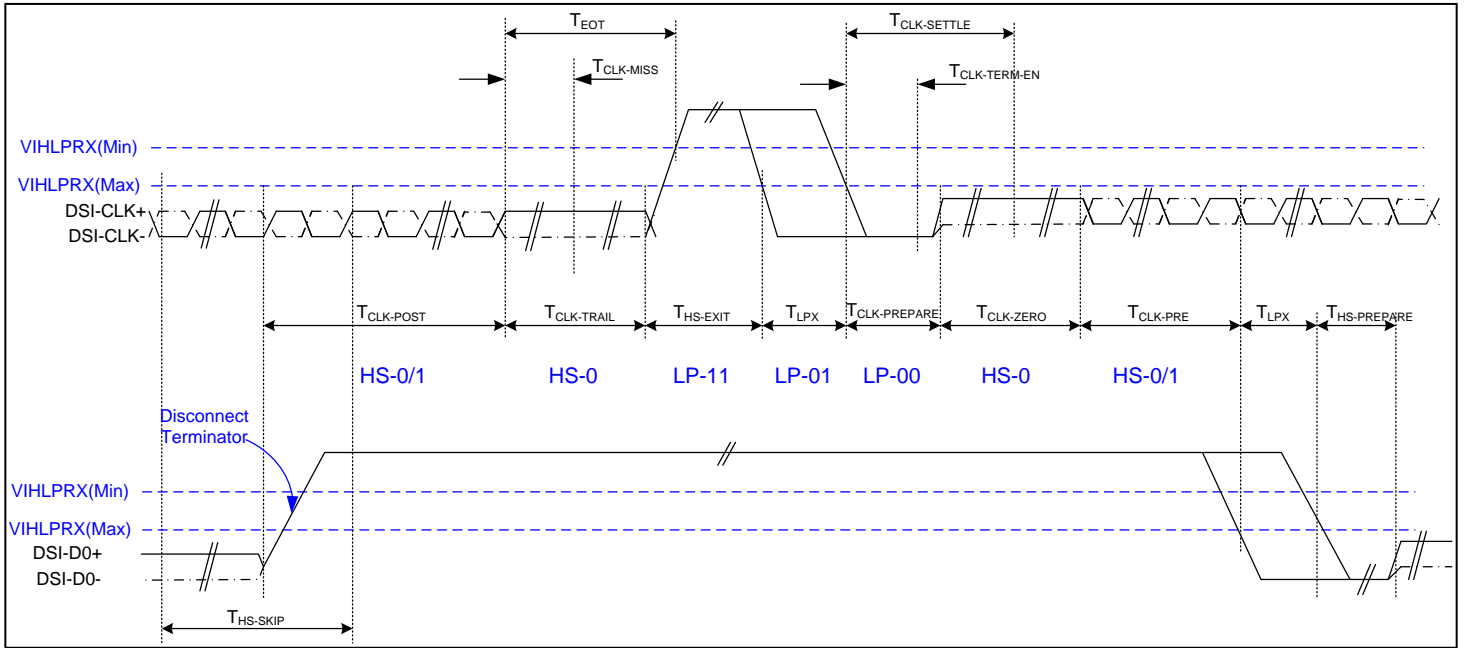
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-DATA_P/N	2xUI INST	Double UI instantaneous	8	25	ns	
DSI-DATA_P/N	UI INSTA ,UI INSTB	UI instantaneous Half	4	12.5	ns	

High-Speed Data Transmission



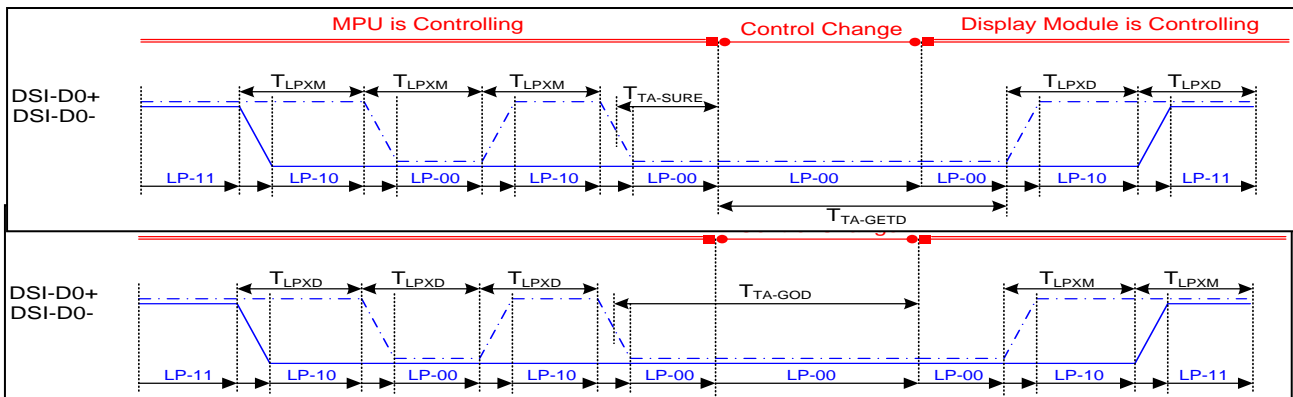
Parameter	Symbol	MIN	TYP	MAX	Unit
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable data receiver line termination measured from when Dn crosses VILMAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode



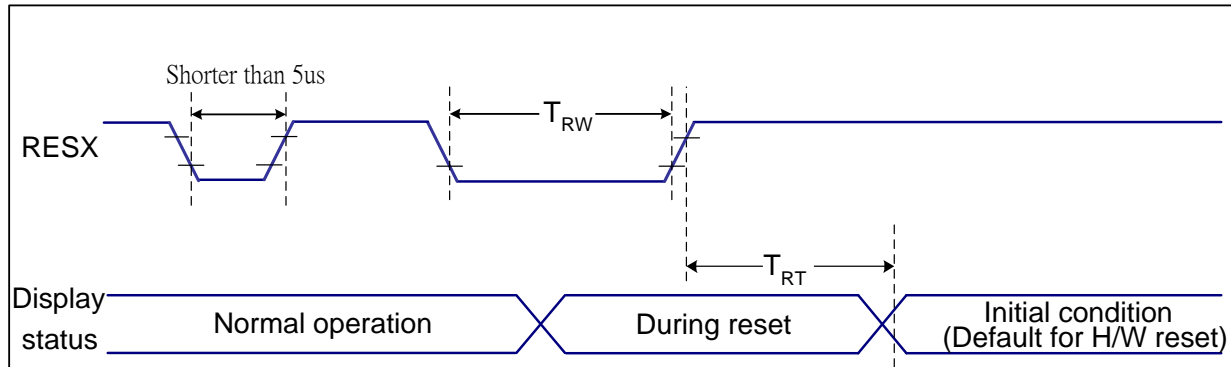
Parameter	Symbol	MIN	TYP	MAX	Unit
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52UI			ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$			60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38		95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	300			ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			38	ns
Minimum time that the HS clock must be set prior to any associated data lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8			UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60			ns

Bus Turnaround Procedure



Parameter	Symbol	MIN	TYP	MAX	Unit
Length of any Low-Power state period : Master side	T _{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T _{LPX}	47.5	50	52.5	ns
Ratio of T _{LPX} (MASTER)/ T _{LPX} (SLAVE) between Master and Slave side	Ratio T _{LPX}	2/3		3/2	
Time-out before new TX side start driving	T _{TA-SURE}	T _{LPX}		2 T _{LPX}	ns
Time to drive LP-00 by new TX	T _{TA-GET}		5 T _{LPX}		ns
Time to drive LP-00 after Turnaround Request	T _{TA-GO}		4 T _{LPX}		ns

7.4.7 Reset Timing



VDDI=1.8V, VDD=2.8V, GND=RGND=0V, T_a=25°C

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
			-	120 (Note 1, 6, 7)	ms

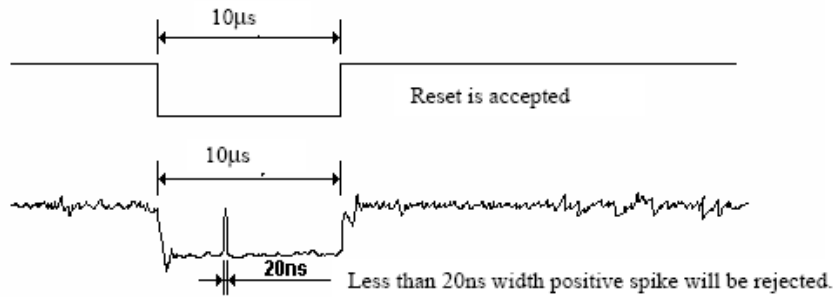
Notes:

- The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
- Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8 INTERFACE

8.1 MPU Interface Type Selection

ST77916 supports 8 bit parallel data bus for 8080 series CPU, RGB serial interfaces, SPI interface, QSPI interface, MIPI interface. Selection of these interfaces are set by IM[2:0] pins as shown below.

IM2	IM1	IM0	Interface	Read Back Data Bus Selection
0	0	0	3-line 9bit serial I/F	SDA: in/out
0	0	1	MIPI I/F_3-line 9bit serial I/F	SDA: in/out · DP · DN
0	1	0	2 data lane serial I/F	SDA1: in/out · SDA2: in
0	1	1	QSPI I/F	SDA[3:0]: in/out
1	0	0	RGB_3-line 9bit serial I/F	SDA: in/out · DB[5:0]
1	0	1	RGB_4-line 8bit serial I/F	SDA: in/out · DB[5:0]
1	1	0	4-line 8bit serial I/F	SDA: in/out
1	1	1	80-8bit parallel I/F	DB[7:0]

Table 6 Interface Type Selection

8.2 8080- I Series MCU Parallel Interface

The MCU can use 8080-8bits parallel interface: 11-lines with 8-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write enable, RDX is the parallel data read enable and D[7:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[7:0] bits is either display data or command parameter. When D/C='0', D[7:0] bits is command. The interface functions of 8080-8bits parallel interface are given in following table.

IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Read back selection
1	1	1	8-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
				1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
				1	↑	1	Read 8-bit display data (D7 to D0)
				1	↑	1	Read 8-bit parameter or status (D7 to D0)

Table 7 the function of 8080 - 8 bits parallel interface

8.2.1 Write cycle sequence

The write cycle means that the host writes information (command / data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (DCX, RDX, WRX) and data signals (DB[7:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (= '0') and vice versa it is data (= '1').

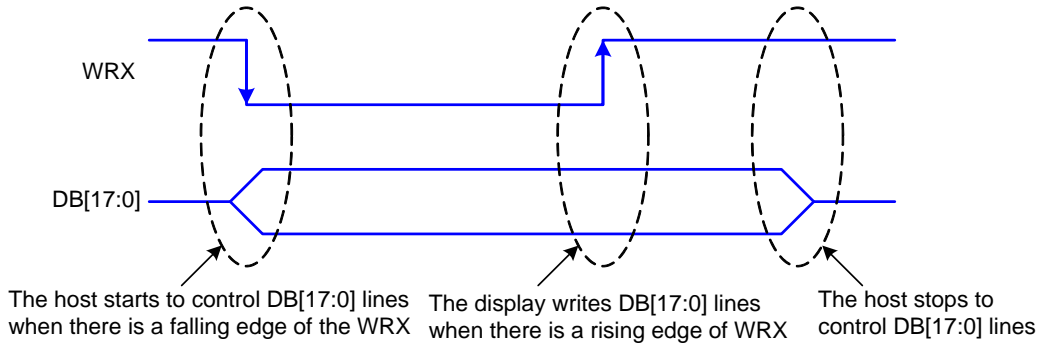


Figure 8 8080 - 8 bits WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped).

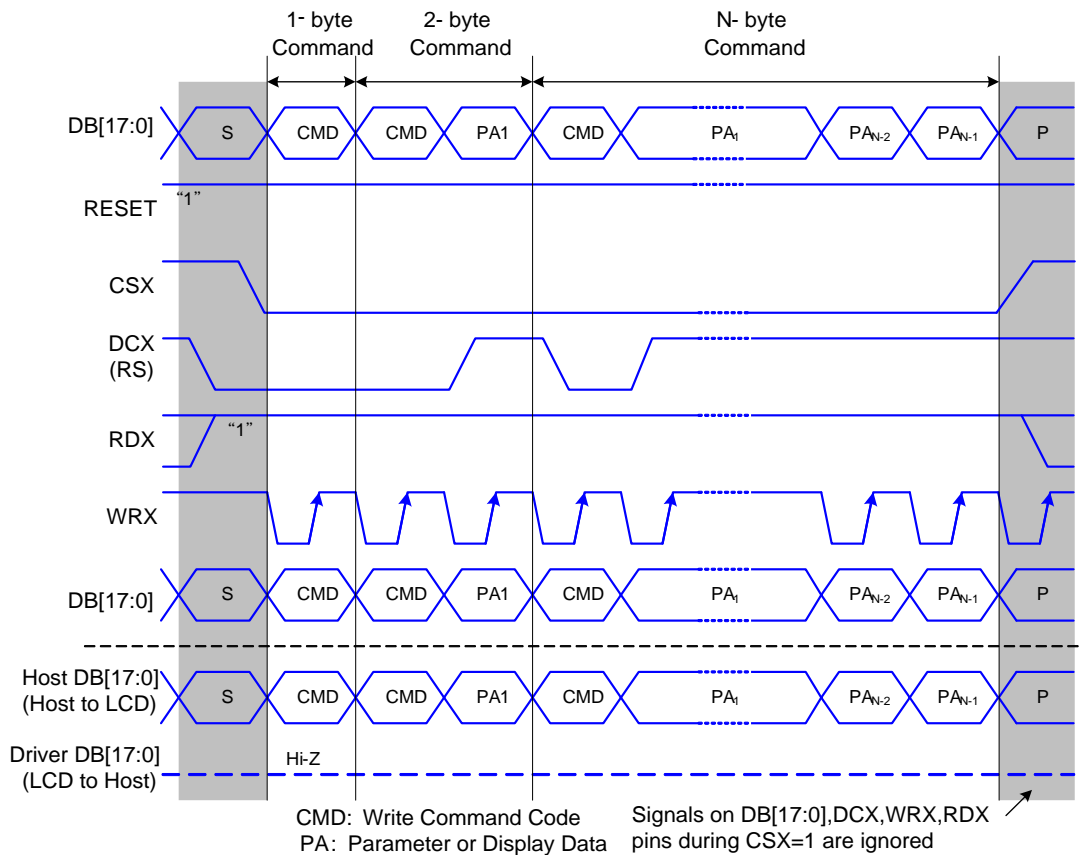


Figure 9 8080 - 8 bits Parallel Bus Protocol, Write to Register or Display RAM

8.2.2 Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[7:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

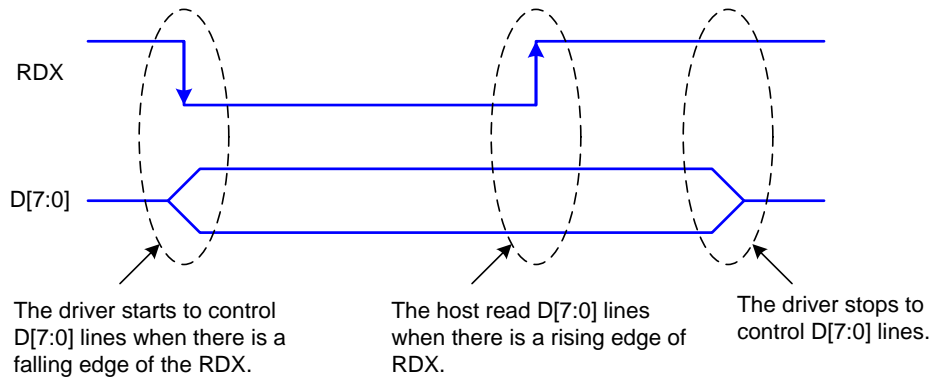


Figure 10 8080 – 8 bits RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).

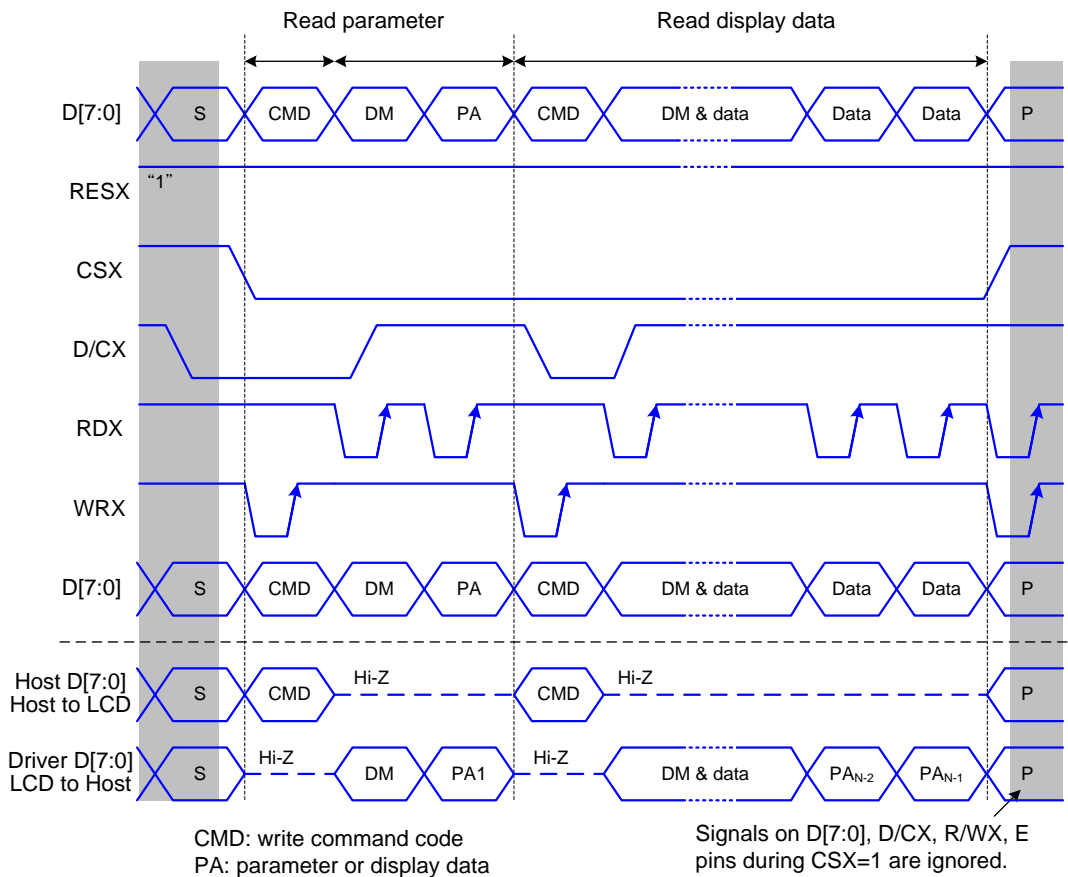


Figure 11 8080 - 8 bits parallel bus protocol, read data from register or display RAM

8.3 Serial Interface

IM2	IM1	IM0	Interface	Read back selection
0	0	0	3-line serial interface I	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
1	1	0	4-line serial interface I	

Table 8 Selection of serial interface

The serial interface is either 3-lines/9-bits or 4-lines/8-bits bi-directional interface for communication between the micro controller and the LCD driver. The 3-lines serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-lines serial interface use: CSX (chip enable), D/CX (data/ command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

8.3.1 Pin description

3-line serial interface I

Pin Name	Description
CSXP	Chip selection signal
RDXP (SCLP)	Clock signal
D0P (SDAP)	Serial input/output data

4-line serial interface I

Pin Name	Description
CSXP	Chip selection signal
DCXP (A0)	Data is regarded as a command when DCXP is low Data is regarded as a parameter or data when DCXP is high
RDXP (SCLP)	Clock signal
D0P (SDA)	Serial input/output data

Table 9 pin description of serial interface

8.3.2 Command write mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. In 4-lines serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is "low", the transmission byte is interpreted as a command byte. If D/CX is "high", the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

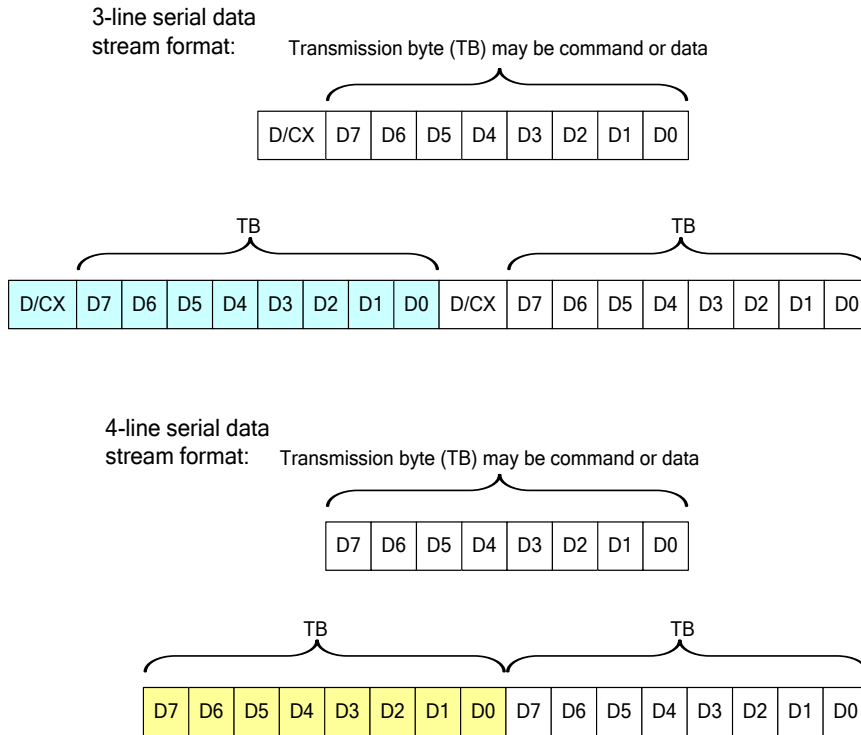


Figure 12 Serial interface data stream format

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX=’0’) or parameter/RAM data (D/CX=’1’). D/CX is sampled when first rising edge of SCL (3-line serial interface) or 8th rising edge of SCL (4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL..

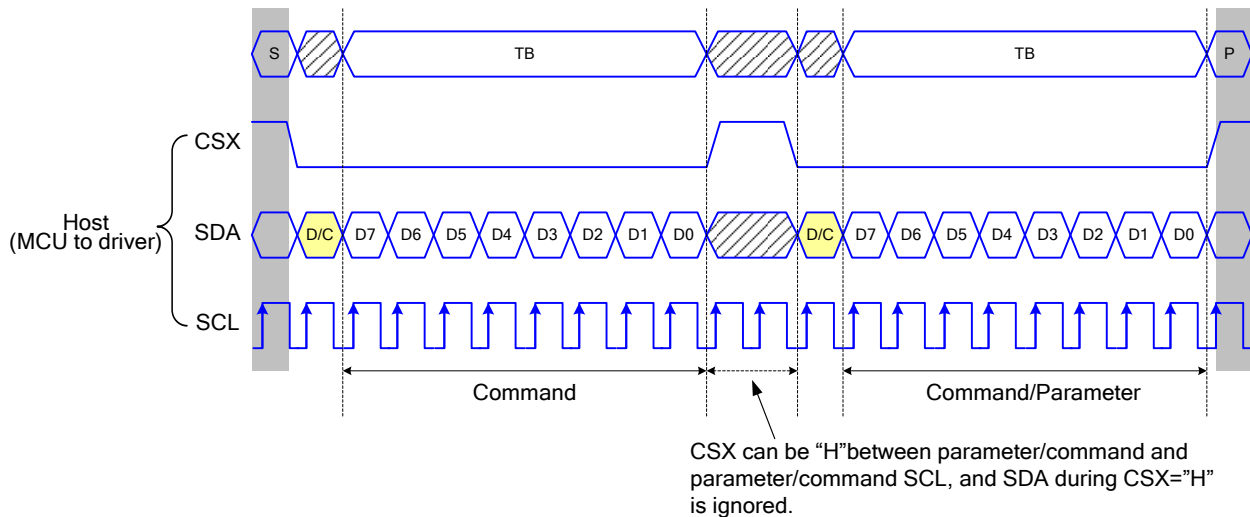


Figure 13 3-line serial interface write protocol (write to register with control bit in transmission)

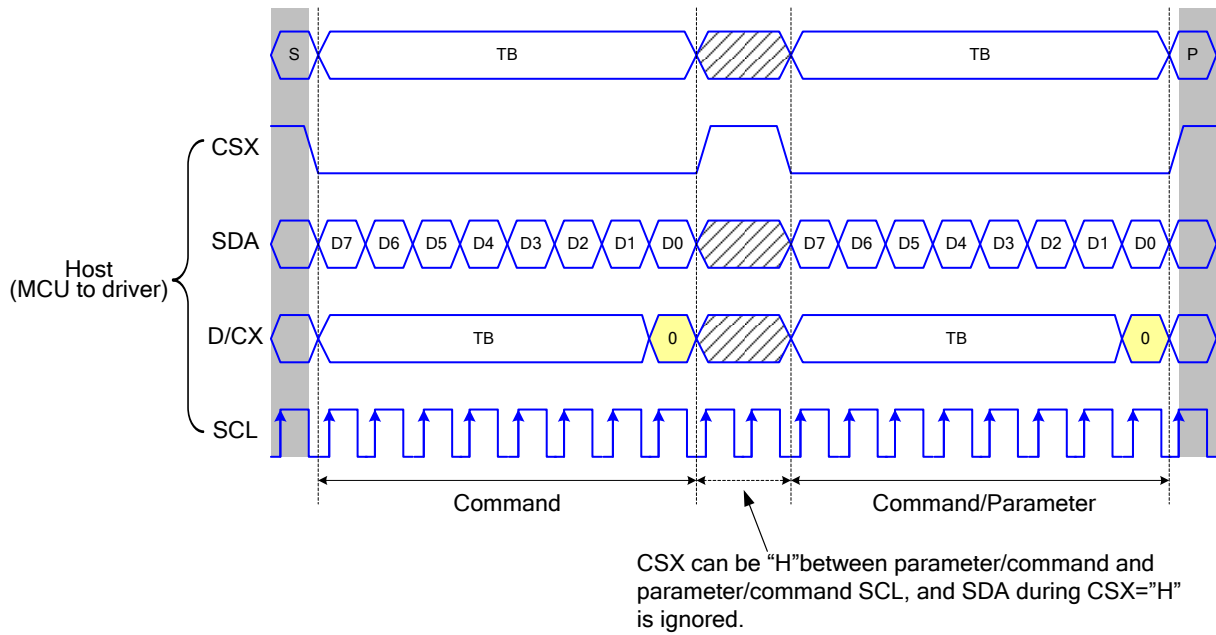


Figure 14 4-line serial interface write protocol (write to register with control bit in transmission)

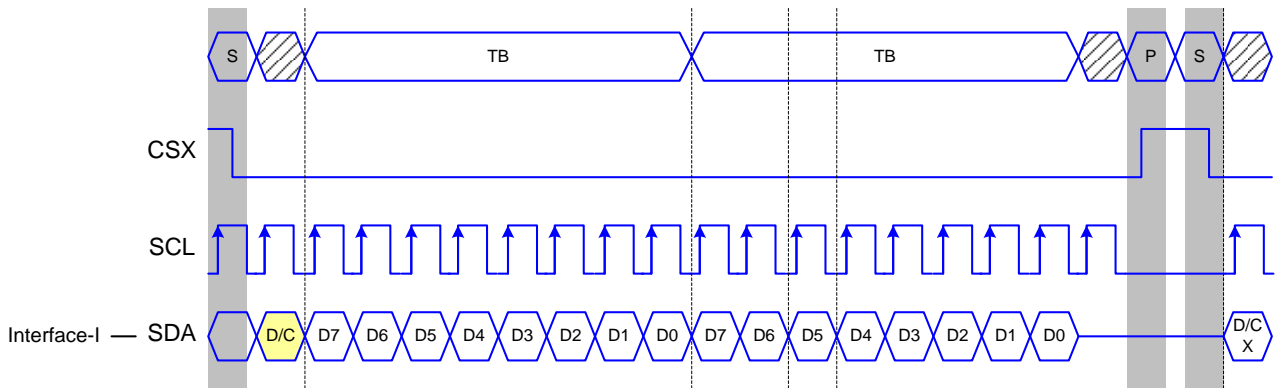
8.3.3 Read function

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

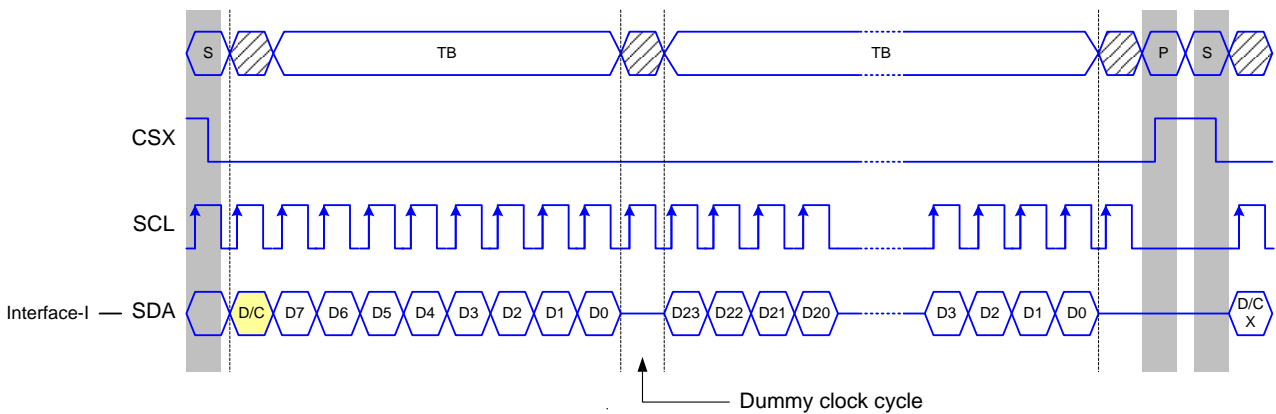
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

8.3.4 3-line serial interface I protocol

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read):



3-line Serial Protocol (for RDDST command: 32-bit read):

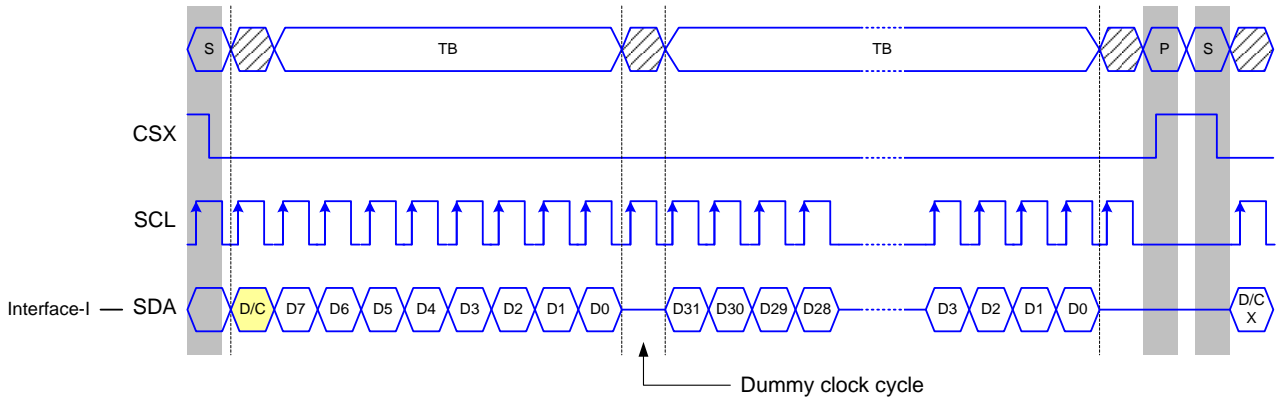
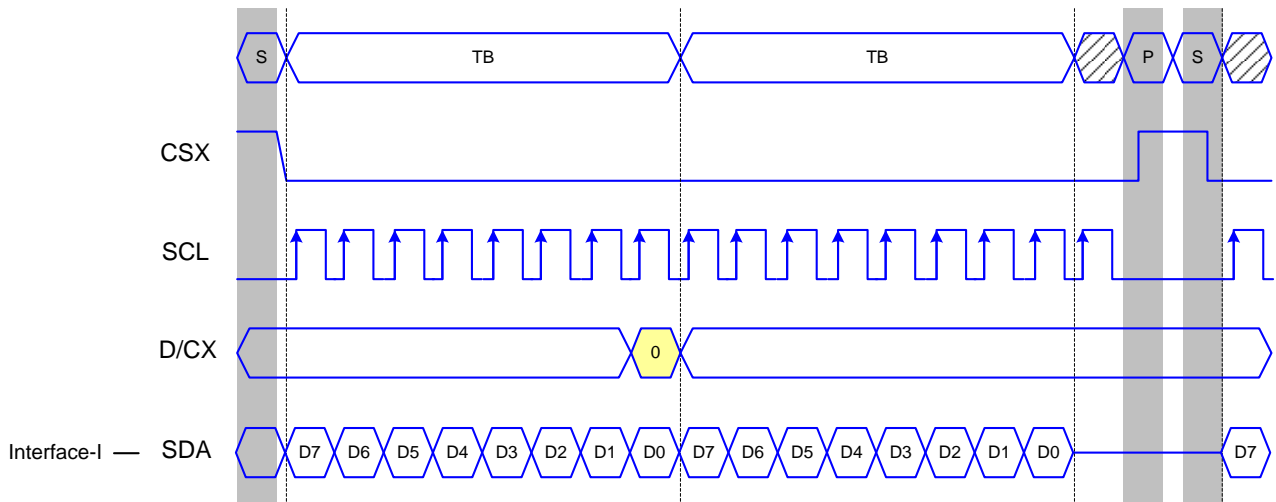


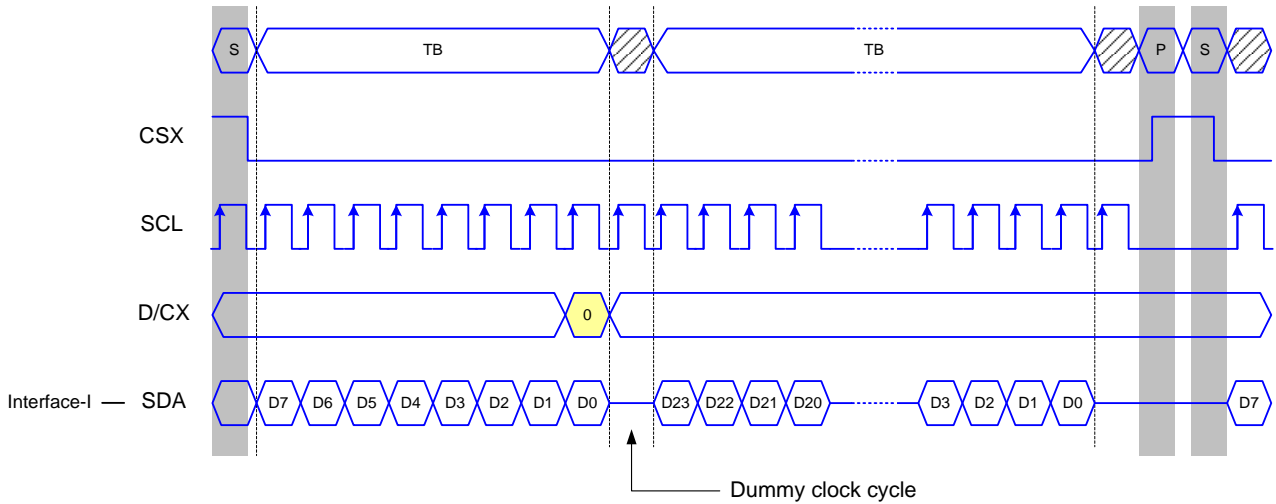
Figure 15 3-line serial interface read protocol

8.3.5 4-line serial protocol

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



4-line serial protocol (for RDDID command: 24-bit read)



4-line Serial Protocol (for RDDST command: 32-bit read)

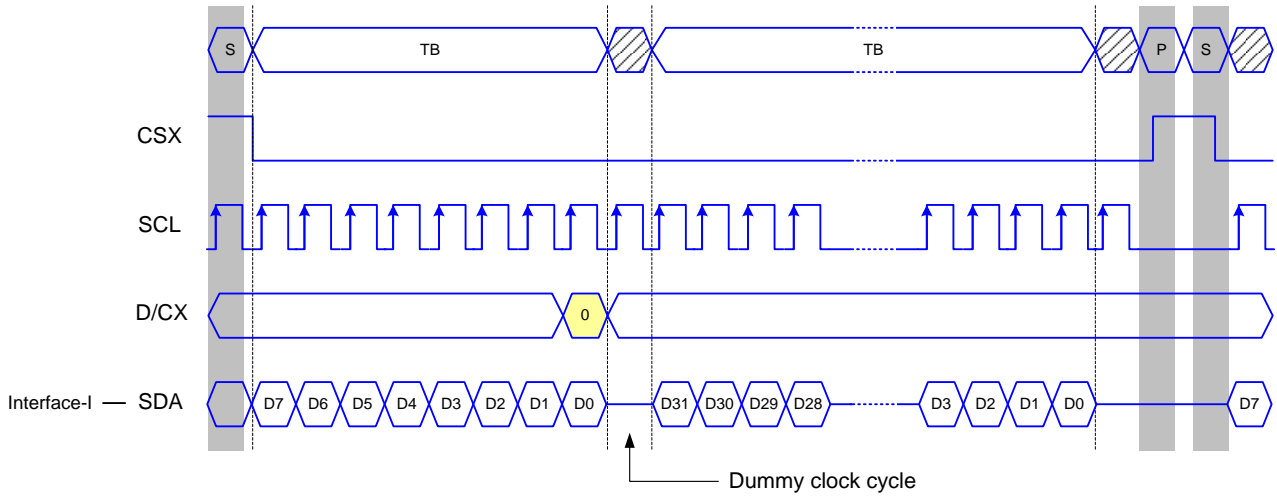


Figure 16 4-line serial interface read protocol

8.4 2 data lane serial Interface

Interface selection:

IM2	IM1	IM0	Interface	Read back selection
0	1	0	2 data lane serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read)

Table 10 IM pin selection

2-wire data lane serial interface use: CSX (chip enable), SCL (serial clock) and SDA1 (serial data input/output 1), and SDA2 (serial data input 2).

2 data lane hardware suggestion and Pin description:

2 data lane serial interface, IM[2:0]=010

2 data lane serial interface

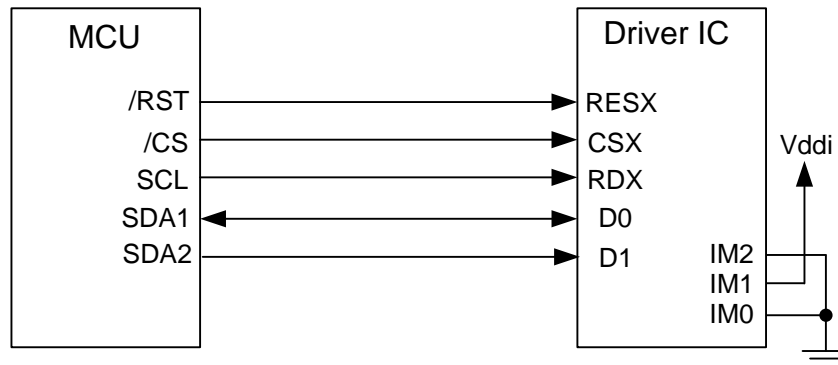


Figure 17 Hardware suggestion of 2 data lane serial interface

Pin Name	Description
CSX	Chip selection signal
RDXP (SCLP)	Clock signal
D0P (SDA1P)	Serial data input/output1
D1P	Serial data input2

Table 11 Pin description of 2 data lane serial interface

Command write mode:

The command write protocol of 2-wire data lane serial interface is the same with the 3-line serial interface, so users can ignore the input data of D1P.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

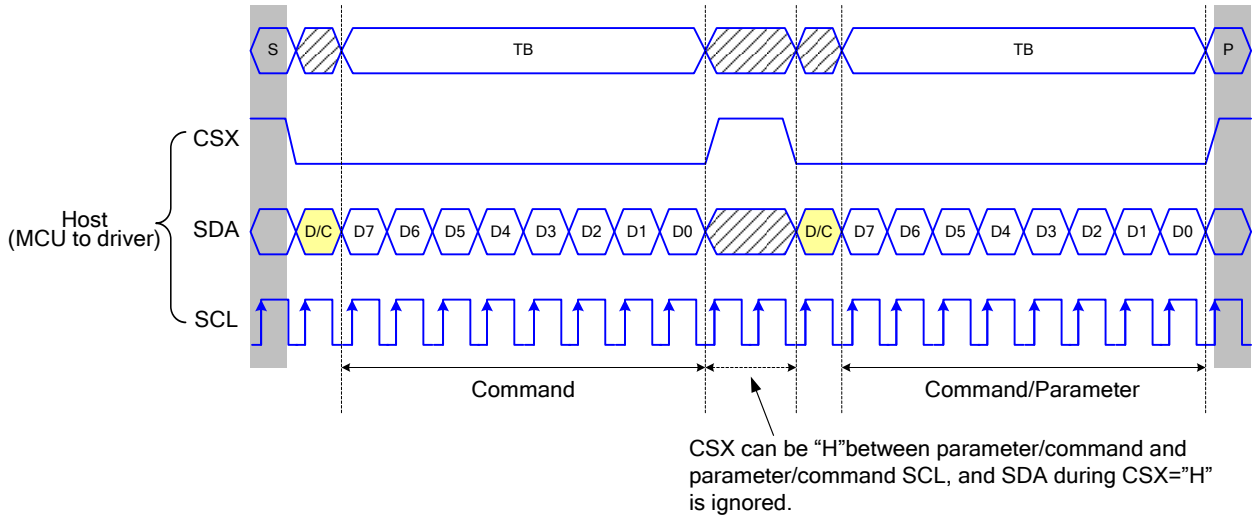


Figure 18 3-line serial interface write protocol (write to register with control bit in transmission)

SRAM write mode:

The SRAM write mode of 2-wire data lane serial interface need use SDA pin and D1P pin to be data input pins.

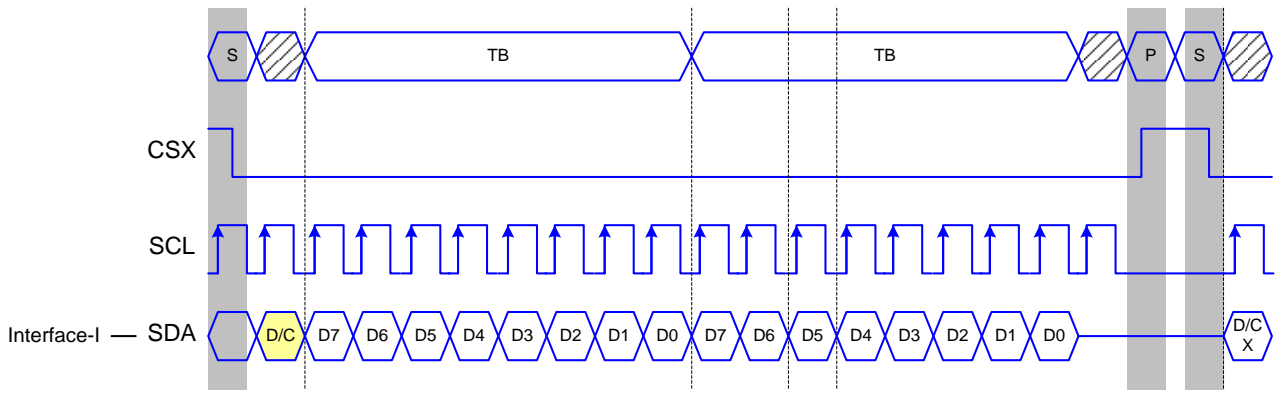
Read function:

The read mode of 2-wire data lane serial interface is the same with the 3-line serial interface and D1P pin can be ignored. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

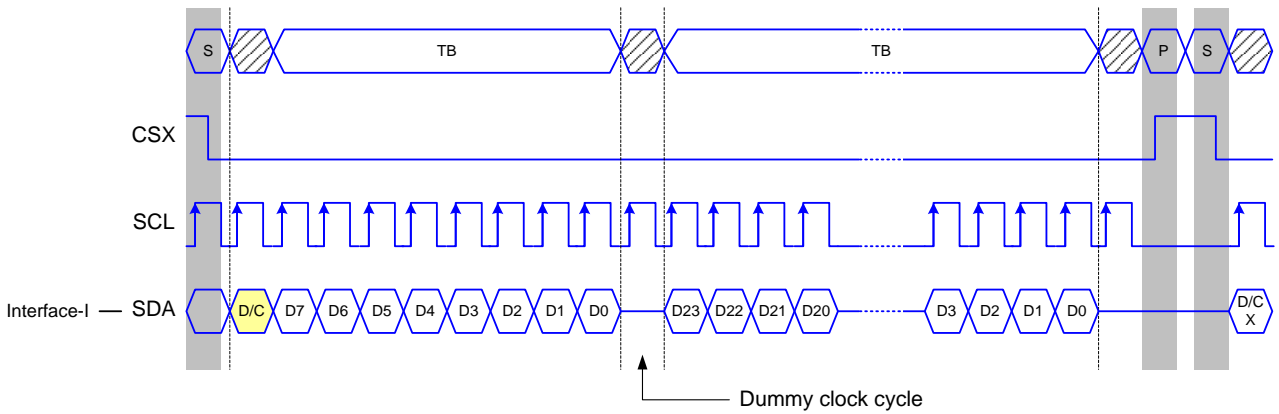
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

3-line serial interface I protocol:

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

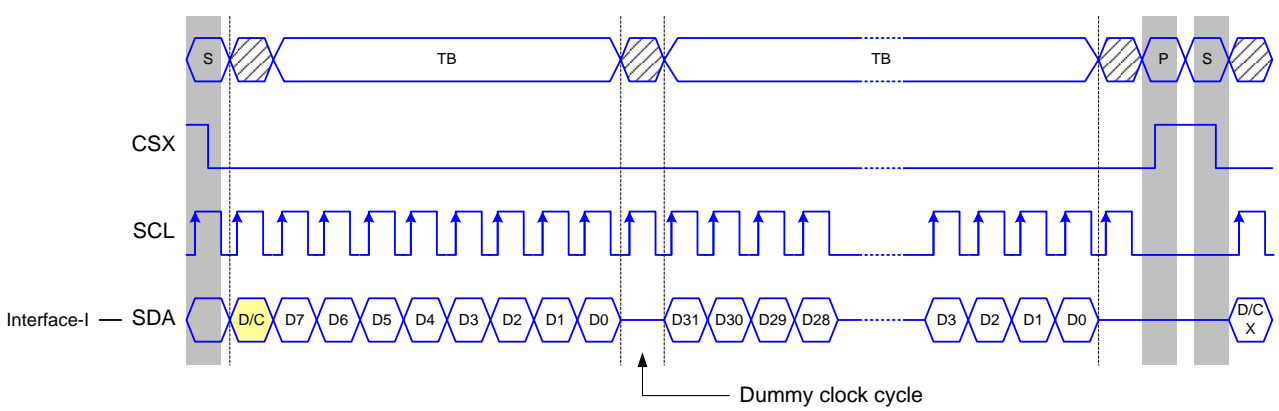


Figure 19 3-line serial interface read protocol

8.5 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state.

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated.

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

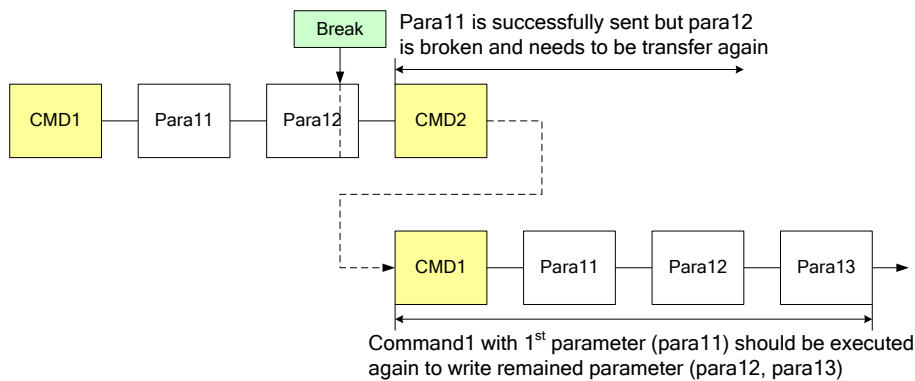


Figure 20 Write interrupts recovery (serial interface)

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

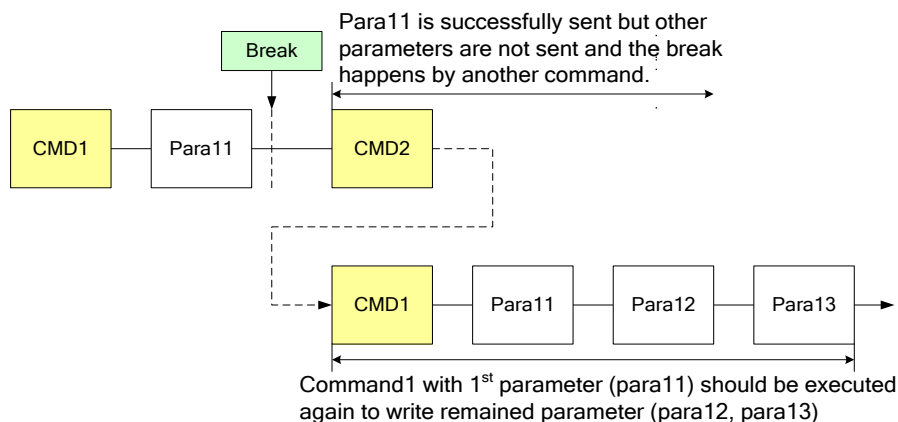


Figure 21 Write interrupts recovery (both serial and parallel Interface)

8.6 Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the Chip Select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the Chip Select line is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the Chip Select line is next enabled as shown below.

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

8.6.1 Parallel interface pause

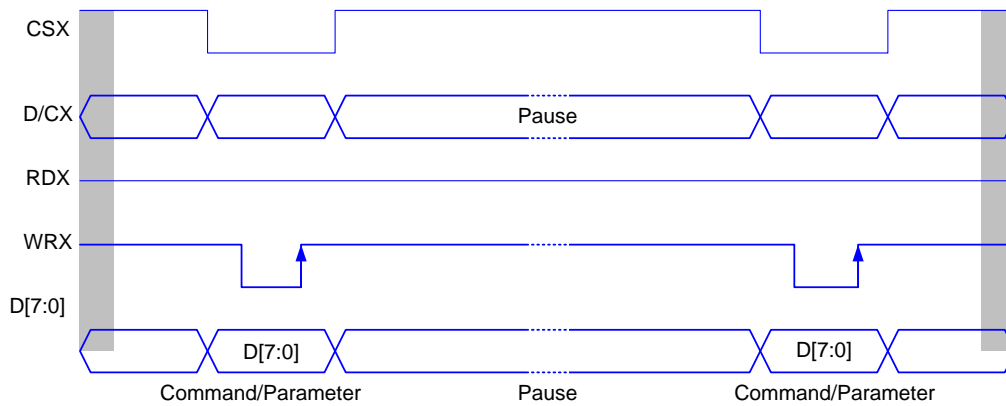


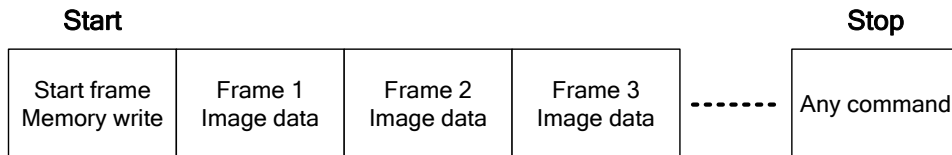
Figure 22 Parallel bus pause protocol (paused by CSX)

8.7 Data Transfer Mode

The module has two kinds color modes for transferring data to the display RAM. These are 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

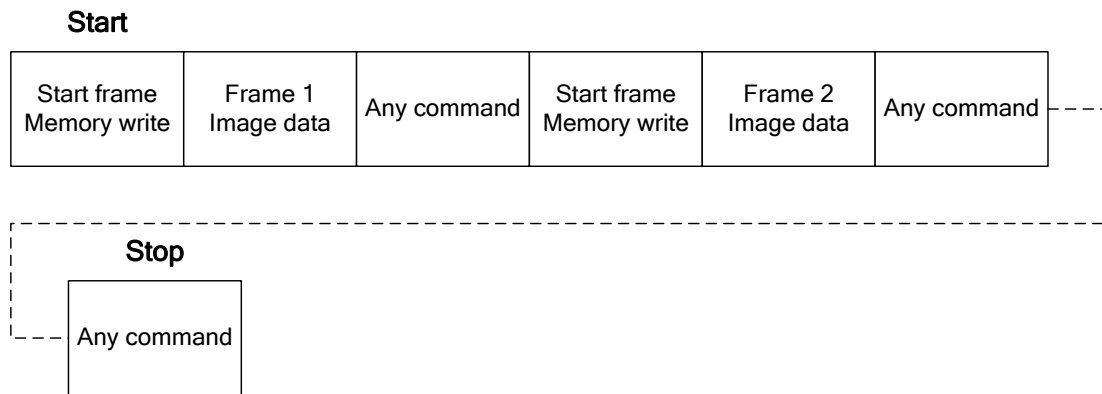
8.7.1 Method 1

The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.



8.7.2 Method 2

The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

8.8 Data Color Coding

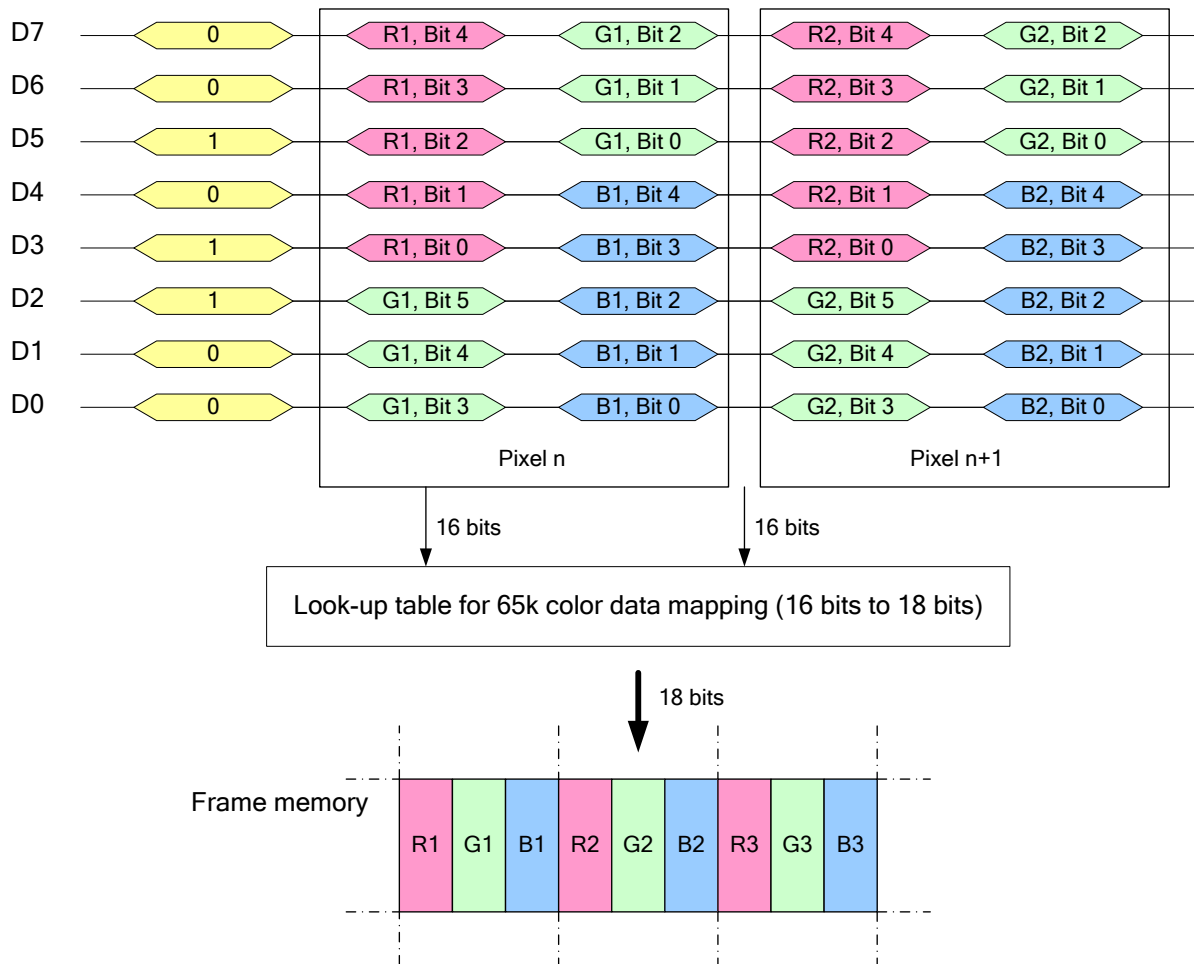
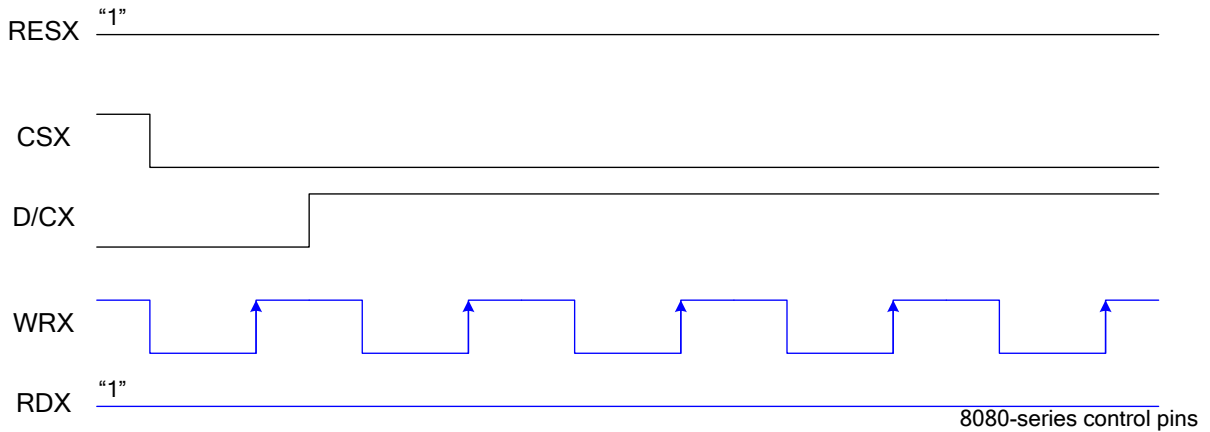
8.8.1 8080- I series 8-bit Parallel Interface

The 8080- I series 8-bit parallel interface of ST77916 can be used by setting IM[2:0]="111b". Different display data formats are available for two Colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

8.8.1.1 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="05h"

There is 1pixel (3 sub-pixels) per 2-byte



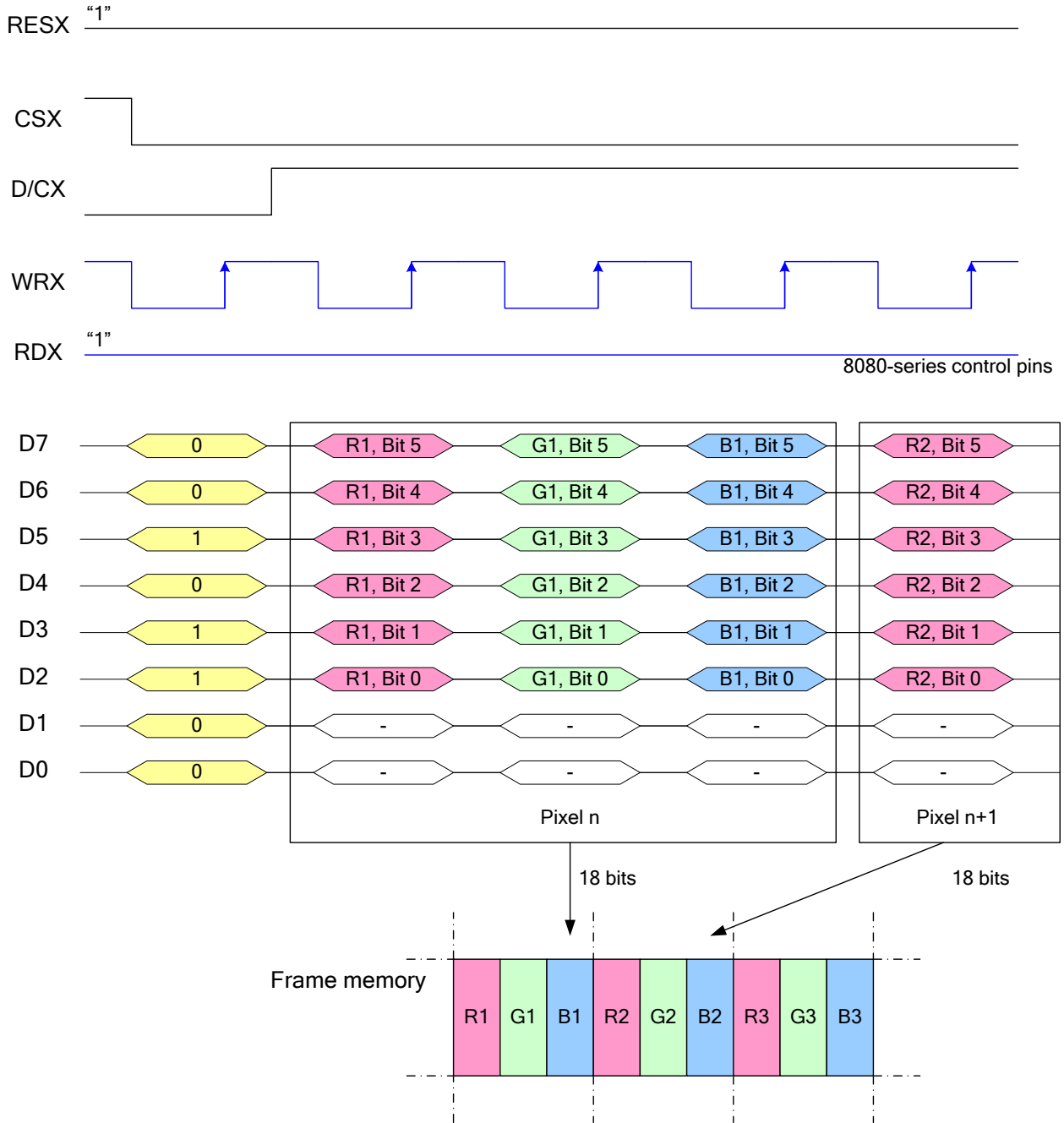
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

8.8.1.2 8-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h"

There is 1pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

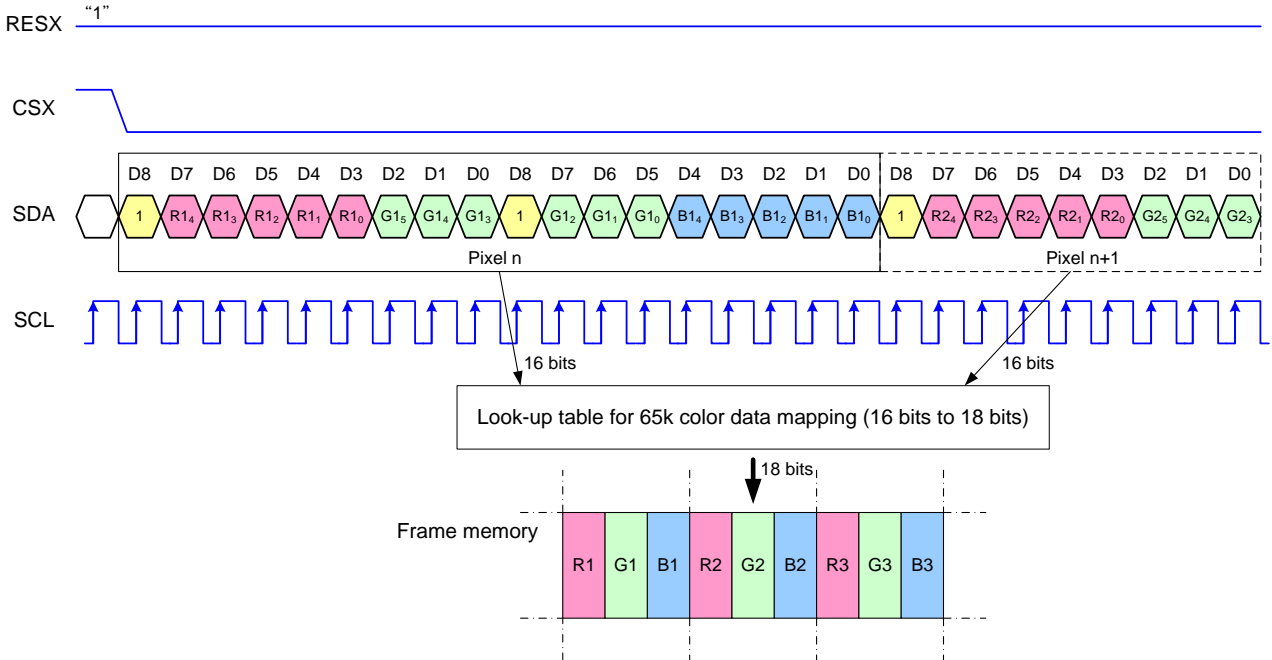
8.8.2 3-Line Serial Interface

Different display data formats are available for two colors depth supported by the LCM listed below.

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

8.8.2.1 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="05h"

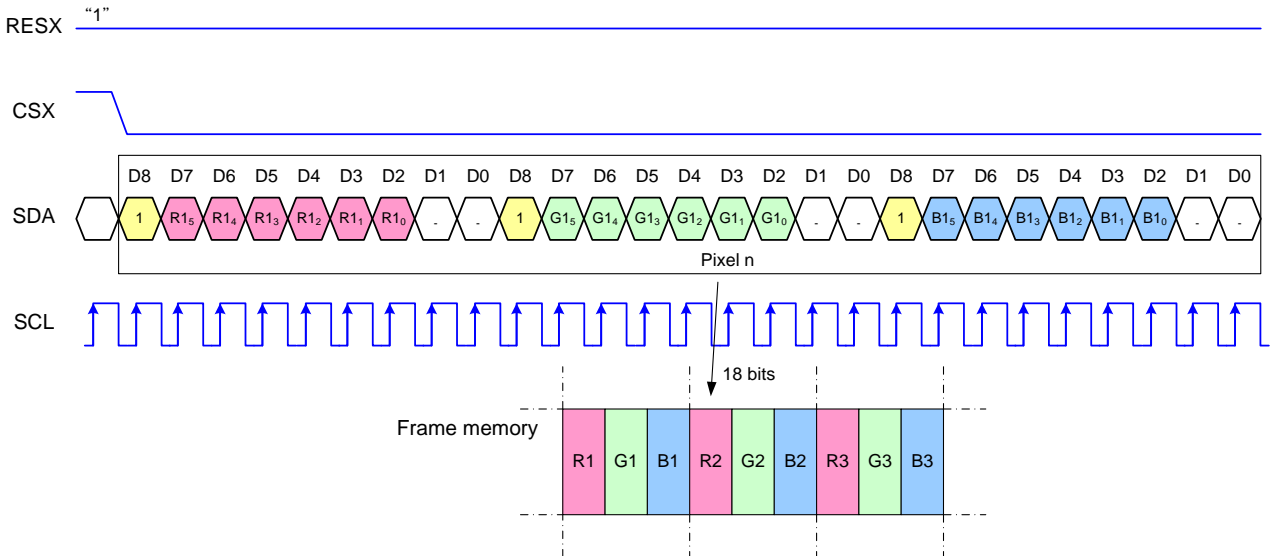


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.8.2.2 Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h"



Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

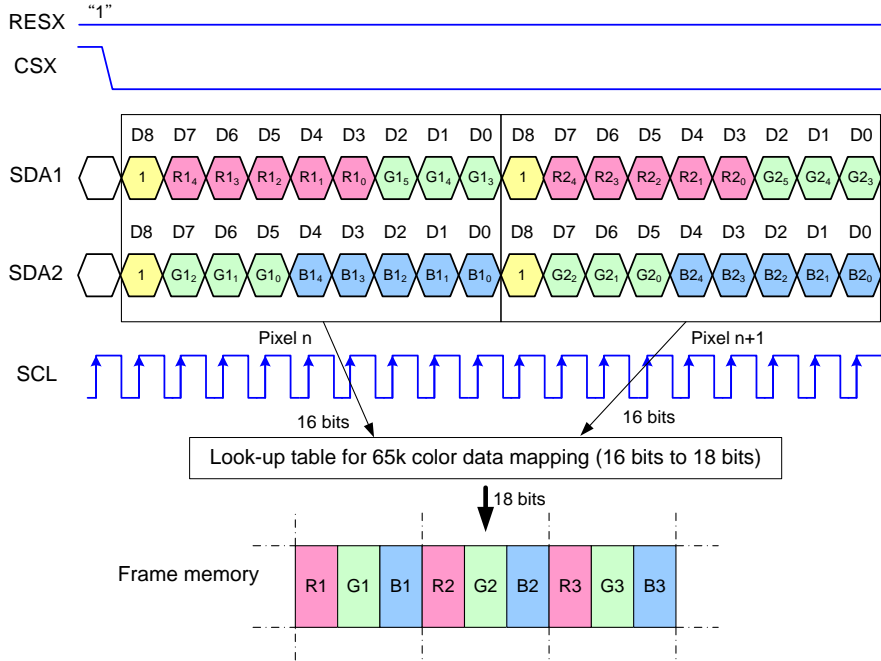
8.8.3 2 Data Lane Serial Interface

Different display data formats are available for two colors depth supported by the LCM listed below.

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

8.8.3.1 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="05h"

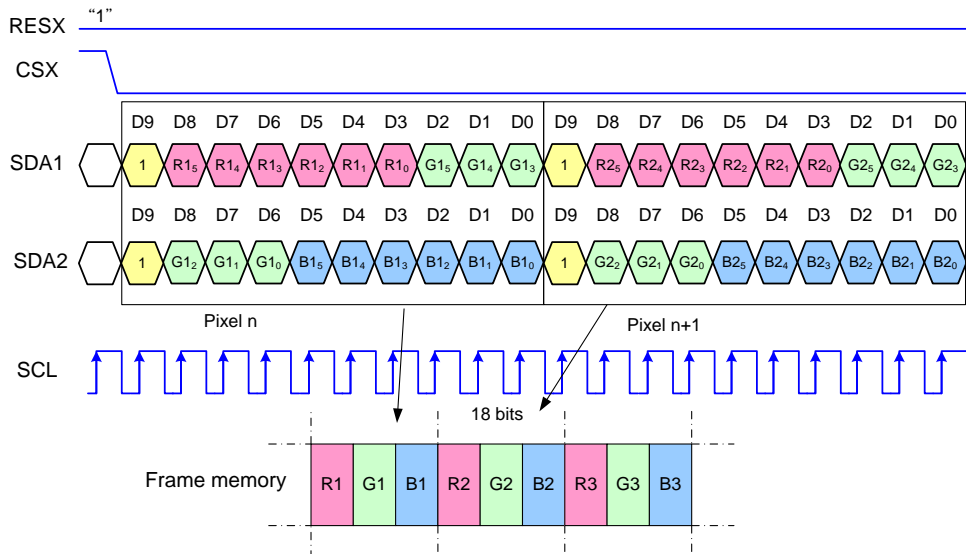


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

8.8.3.2 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3Ah="06h"



Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

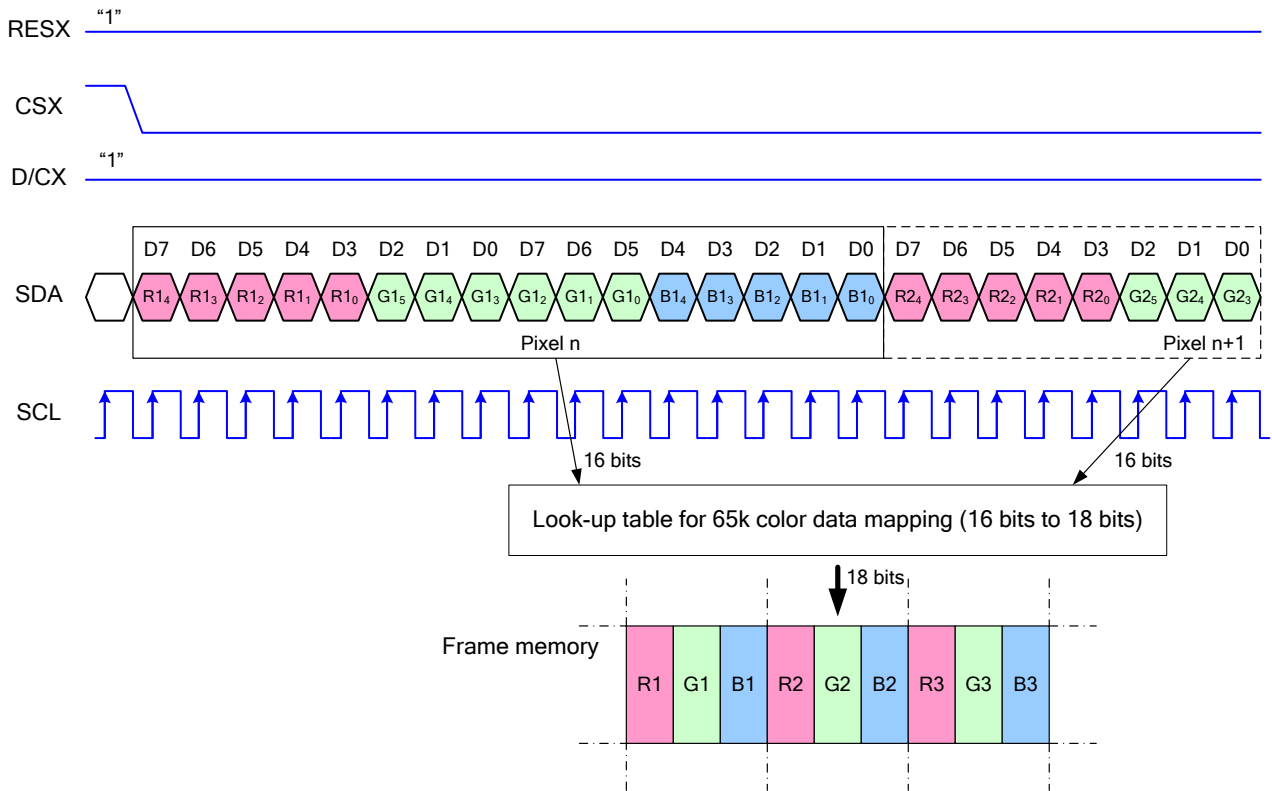
8.8.4 4-Line Serial Interface

Different display data formats are available for two colors depth supported by the LCM listed below.

65k colors, RGB 5-6-5-bit input

262k colors, RGB 6-6-6-bit input

8.8.4.1 Write data for 16-bit/pixel (RGB-5-6-5-bit input), 65K-Colors, 3Ah="05h"

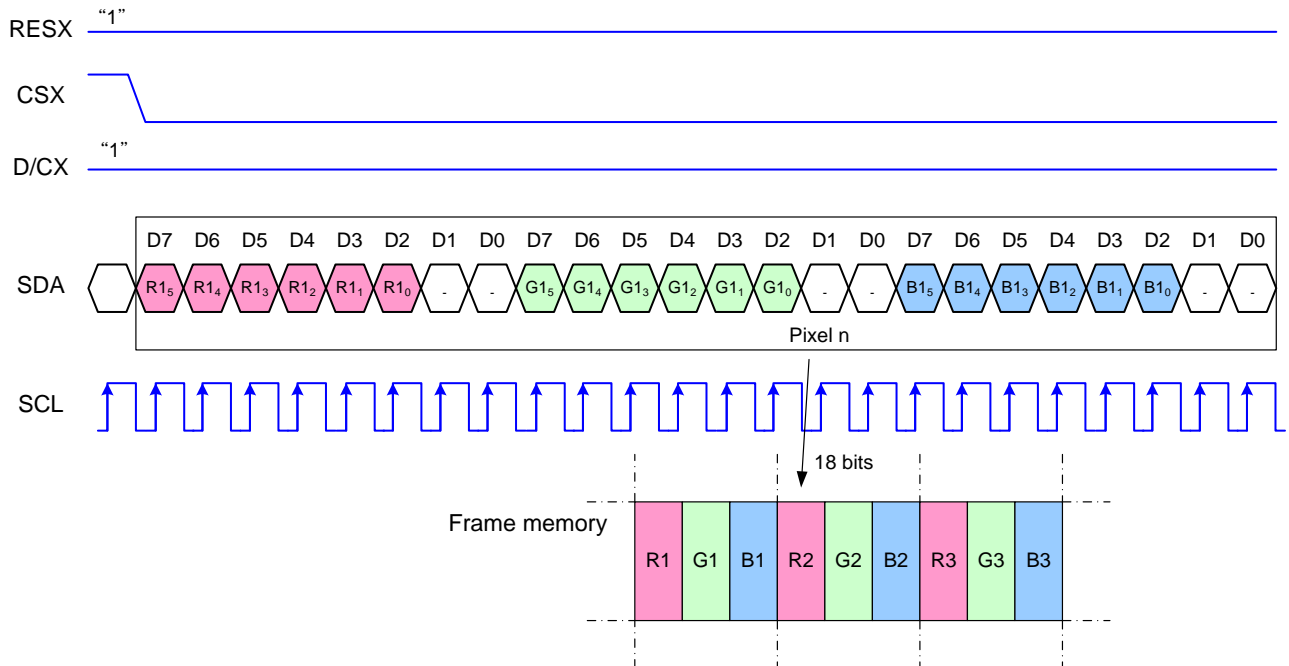


Note 1. Pixel data with the 16-bit color depth information

Note 2. The most significant bits are: Rx4, Gx5 and Bx4

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

8.8.4.2 Write data for 18-bit/pixel (RGB-6-6-6-bit input), 262K-Colors, 3Ah="06h"



Note 1. Pixel data with the 18-bit color depth information

Note 2. The most significant bits are: Rx5, Gx5 and Bx5

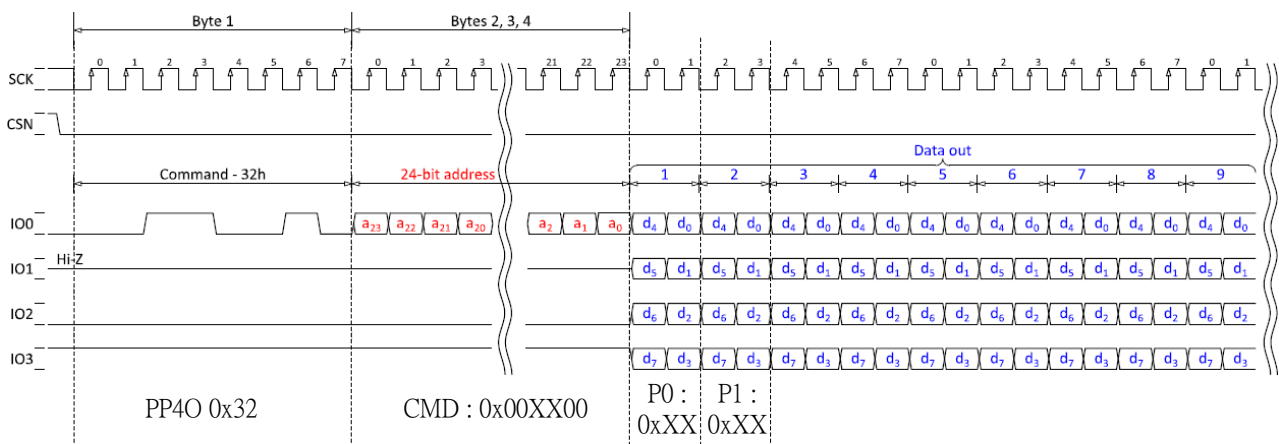
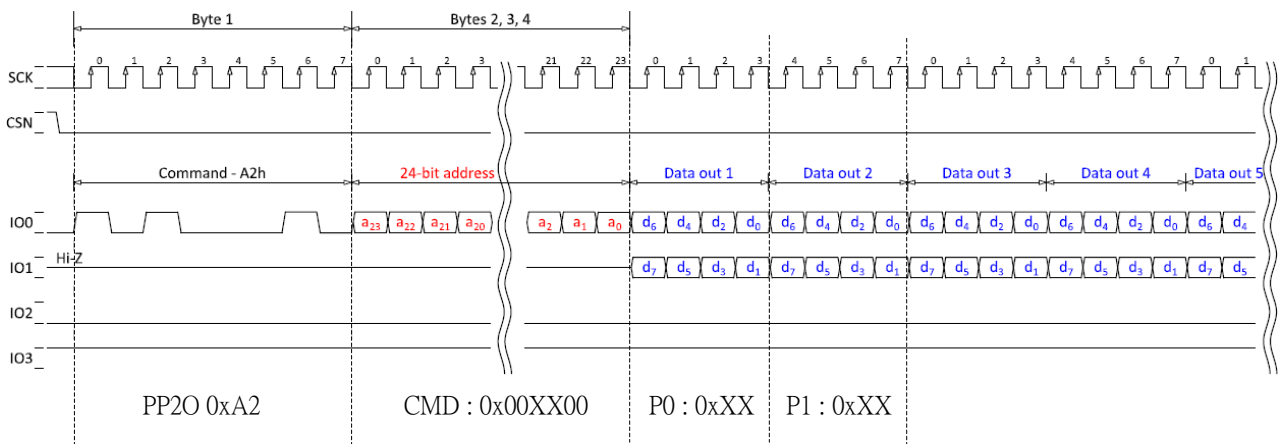
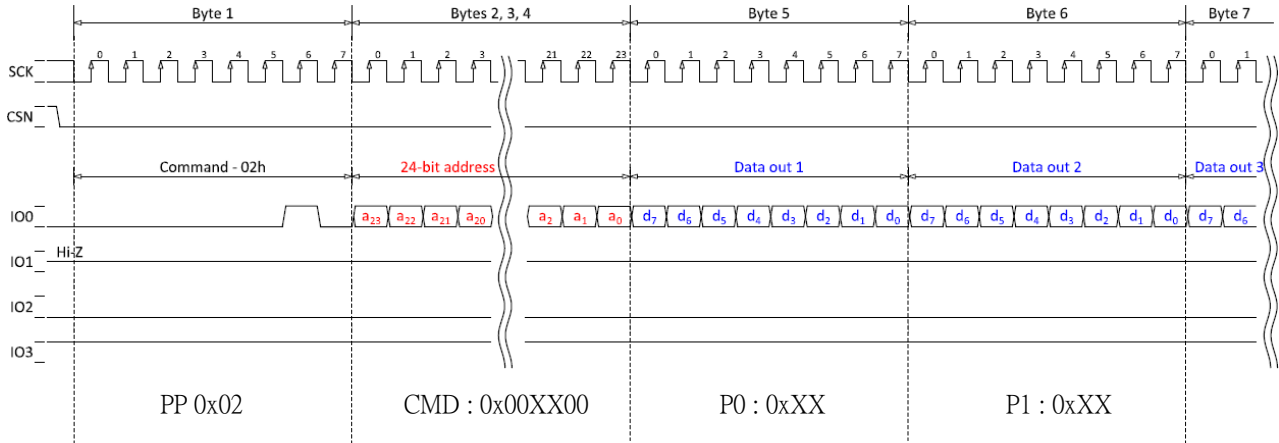
Note 3. The least significant bits are: Rx0, Gx0 and Bx0

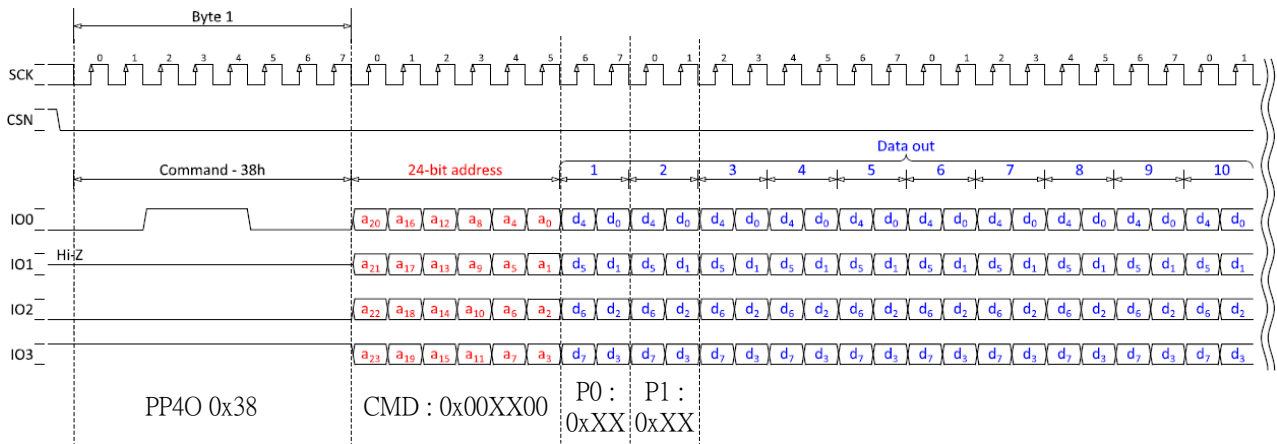
8.8.5 Quad-SPI Interface

Pin Name	Description
CSXP	Chip selection signal
RDXP (SCLP)	Clock signal (Max=50MHz)
D0P	Serial input/output data lane 0
D1P	Serial input data lane 1
D2P	Serial input data lane 2
D3P	Serial input data lane 3

8.8.5.1 Command write mode:

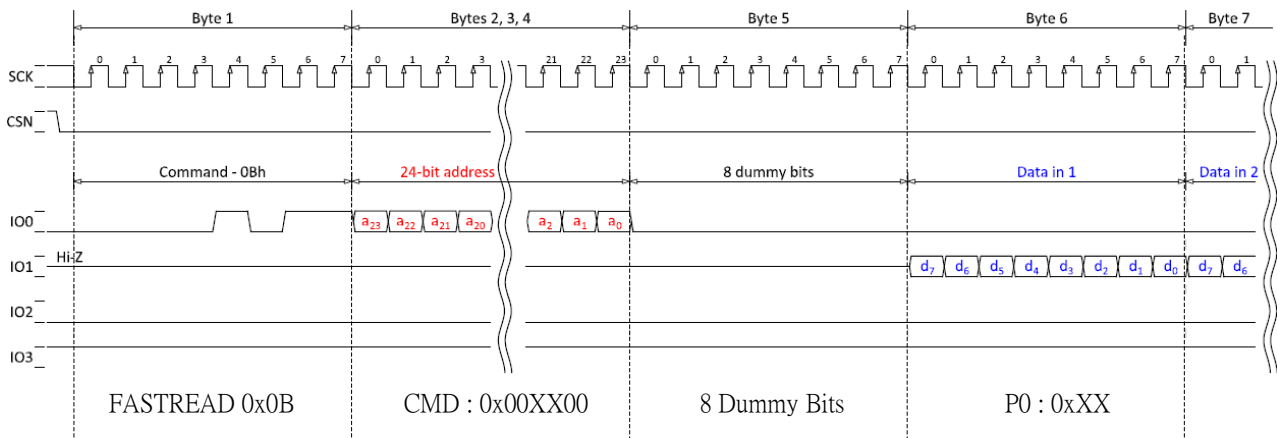
When host writes commands or parameter to ST77916, host needs to send 1 byte of write command instruction (0x02 · 0xA2 · 0x32 or 0x38). Then host sends 3 bytes of AD[23:0] which is composed of 1 byte of 0x00, 1 byte of command address and 1 byte of 0x00. After host sending instruction and AD[23:0], the following data is parameter (are parameters). When the last bit of parameter has been sent, CSX pin should be returned “H” level.





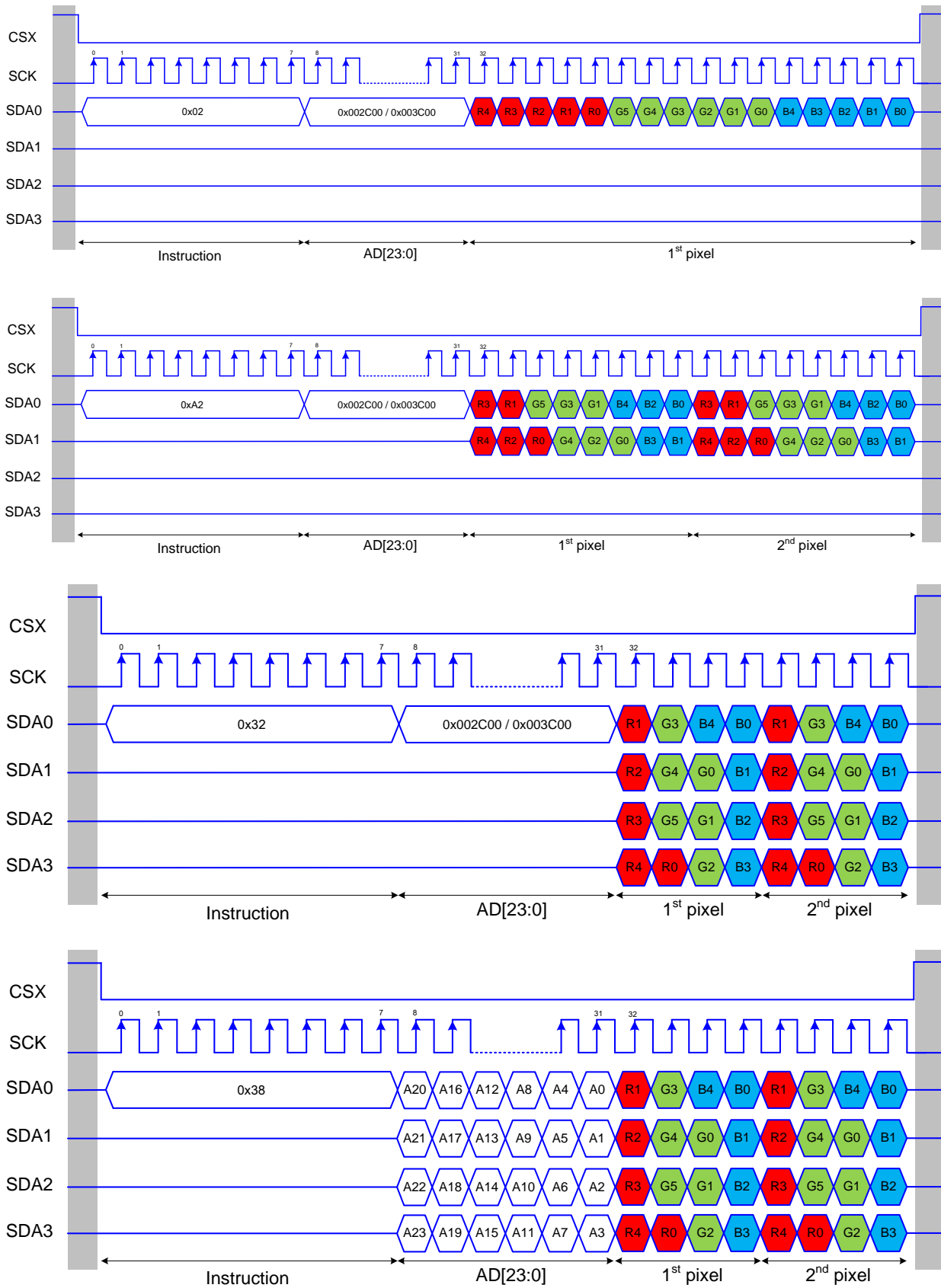
8.8.5.2 Read command mode

When host reads commands or parameter to ST77916, host needs to send 1 byte of write command instruction (0x0B). Then host sends 3 bytes of AD[23:0] which is composed of 1 byte of 0x00, 1 byte of command address and 1 byte of 0x00. After host sending read command and AD[23:0], the following output data is command address parameter (are parameters). When the last bit of parameter has been output, CSX pin should be returned "H" level.

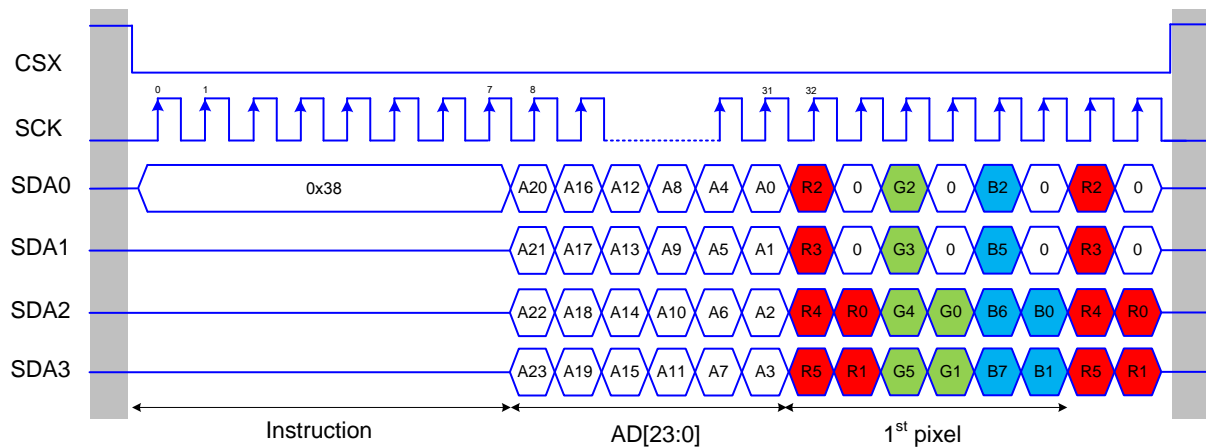
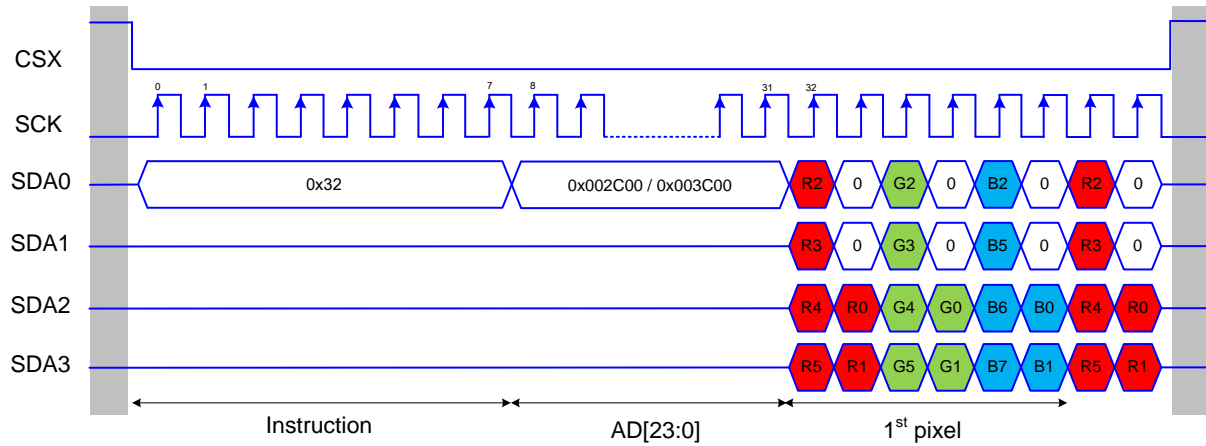
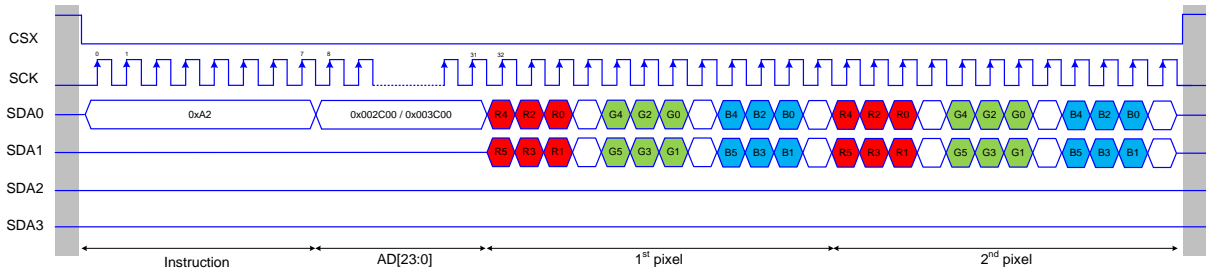
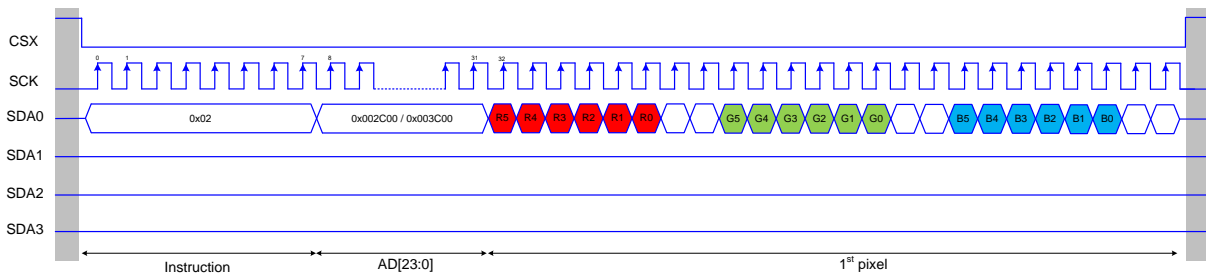


8.8.5.3 Color Format

QSPI RGB565



QSPI RGB666



8.9 RGB Interface

8.9.1 RGB interface Selection

The color format selection of RGB Interface for ST77916 is selected by setting the command 3Ah, DB [6:4].

RGB Interface Mode	3Ah, DB[6:4]	Data pins
6-bit 262K RGB Interface	110	DB[5:0]
6-bit 65K RGB Interface	101	DB[5:0]

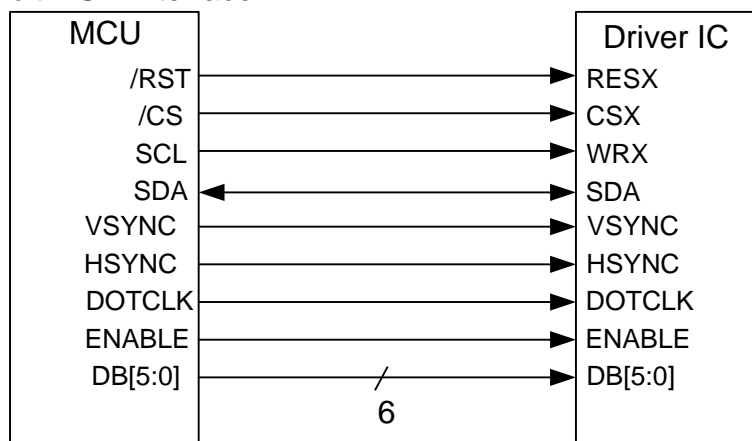
8.9.2 RGB Color Format

ST77916 supports two kinds of RGB interface, DE mode and HV mode, and 6bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[5:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[5:0] pins can be used. When using RGB interface, only serial interface can be selected.

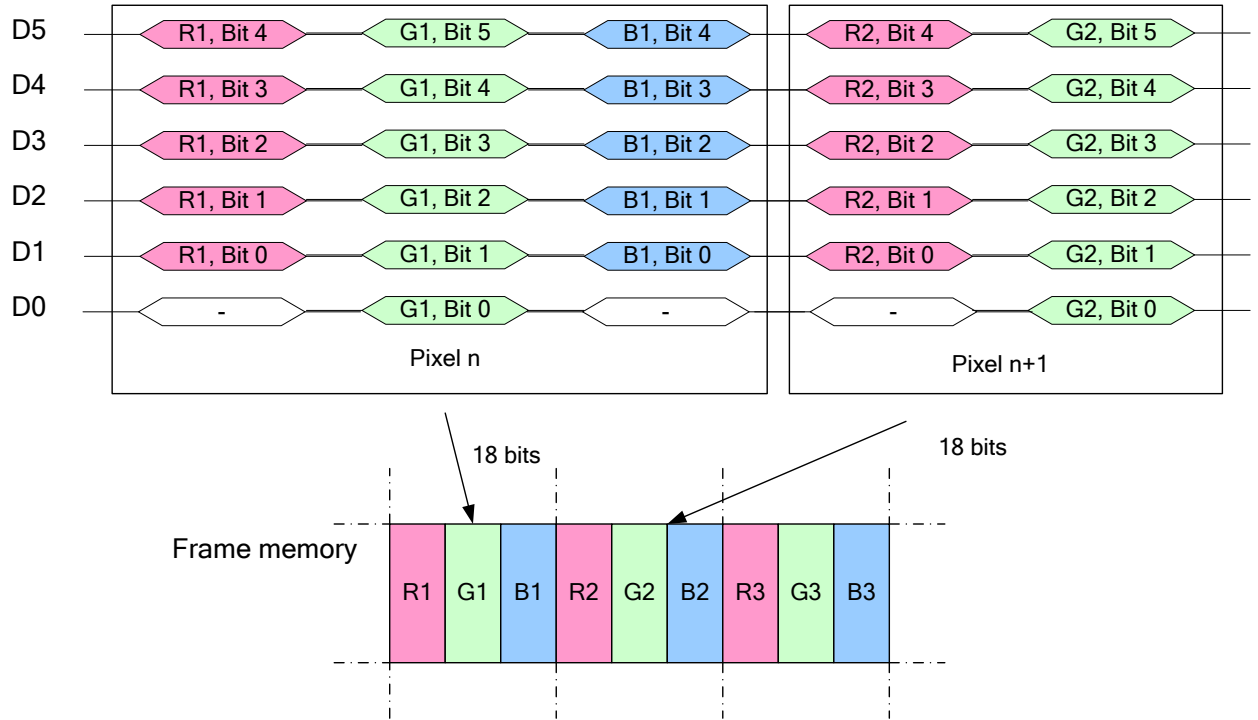
6-bit RGB interface & 3-line serial interface hardware suggestion, IM[2:0]=100.

6-bit RGB interface & 4-line serial interface hardware suggestion, IM[2:0]=101.

6-bit RGB Interface



Write data for 6-bit/pixel (RGB 5-6-5-bit input), 65K-Colors



Write data for 6-bit/pixel (RGB 6-6-6-bit input), 262K-Colors

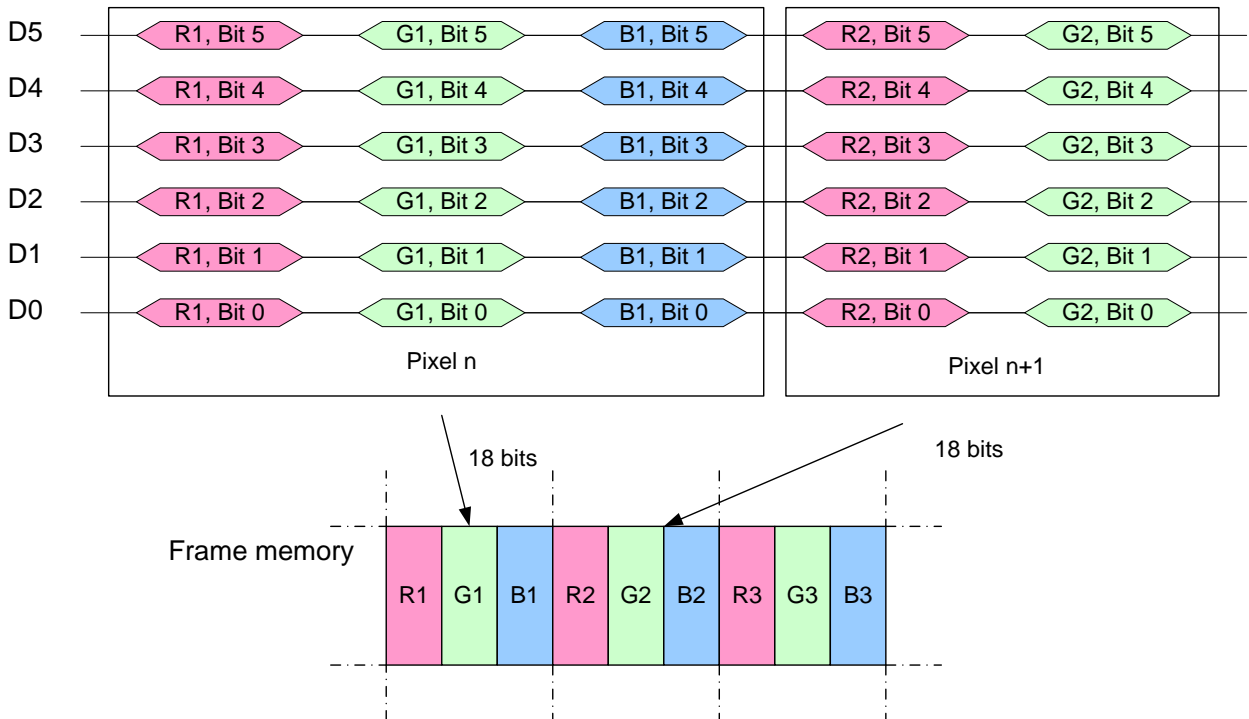


Figure 23 RGB Interface Data Format

8.9.3 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.

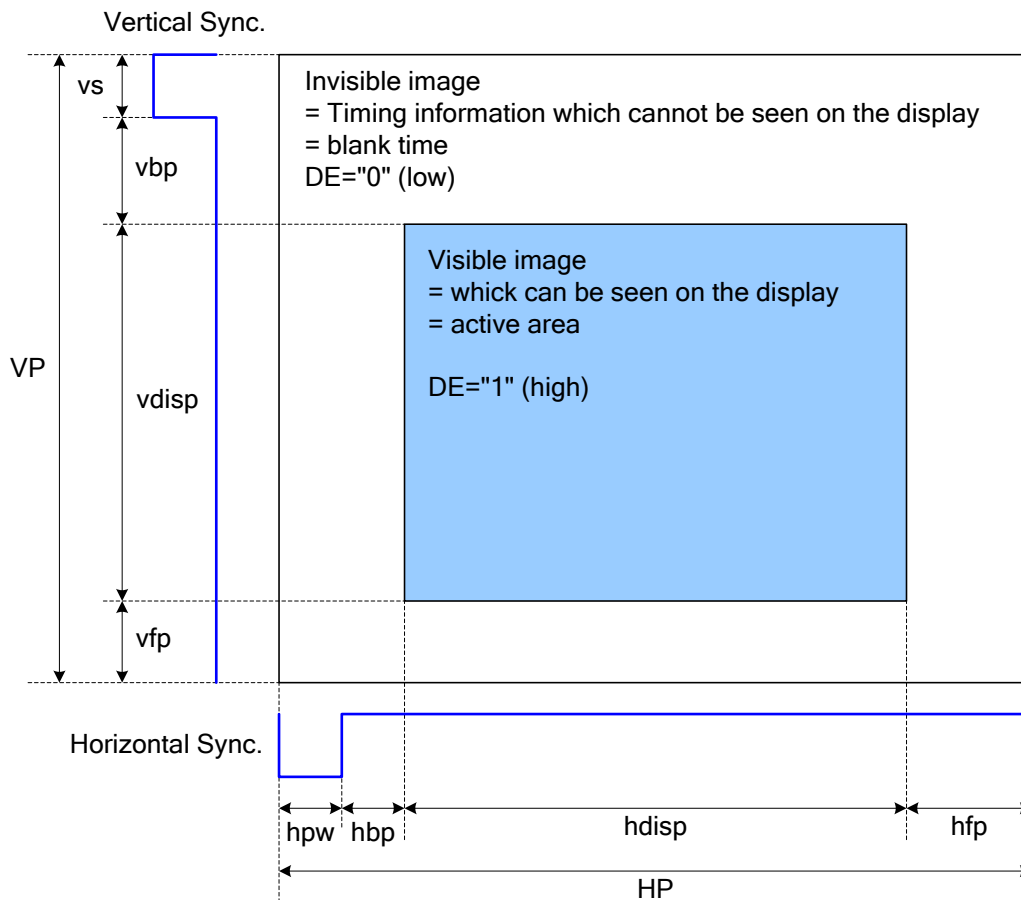


Figure 24 DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

6bit RGB interface:

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	6	30	hpw+hbp=93	Clock
Horizontal Sync. Back Porch	hbp	12	30		Clock
Horizontal Sync. Front Porch	hfp	6	60	-	Clock
Vertical Sync. Width	vs	2	4	vs+vbp=127	Line
Vertical Sync. Back Porch	vbp	2	4		Line
Vertical Sync. Front Porch	vfp	2	8	-	Line

Note:

Typical value are related to the setting of dot clock is 17MHz and frame rate is 60Hz, VDD=VDDI=2.8V..

In with ram mode, $hpw+hbp+hfp \geq 66$

In without ram mode, $hpw+hbp \geq 60$

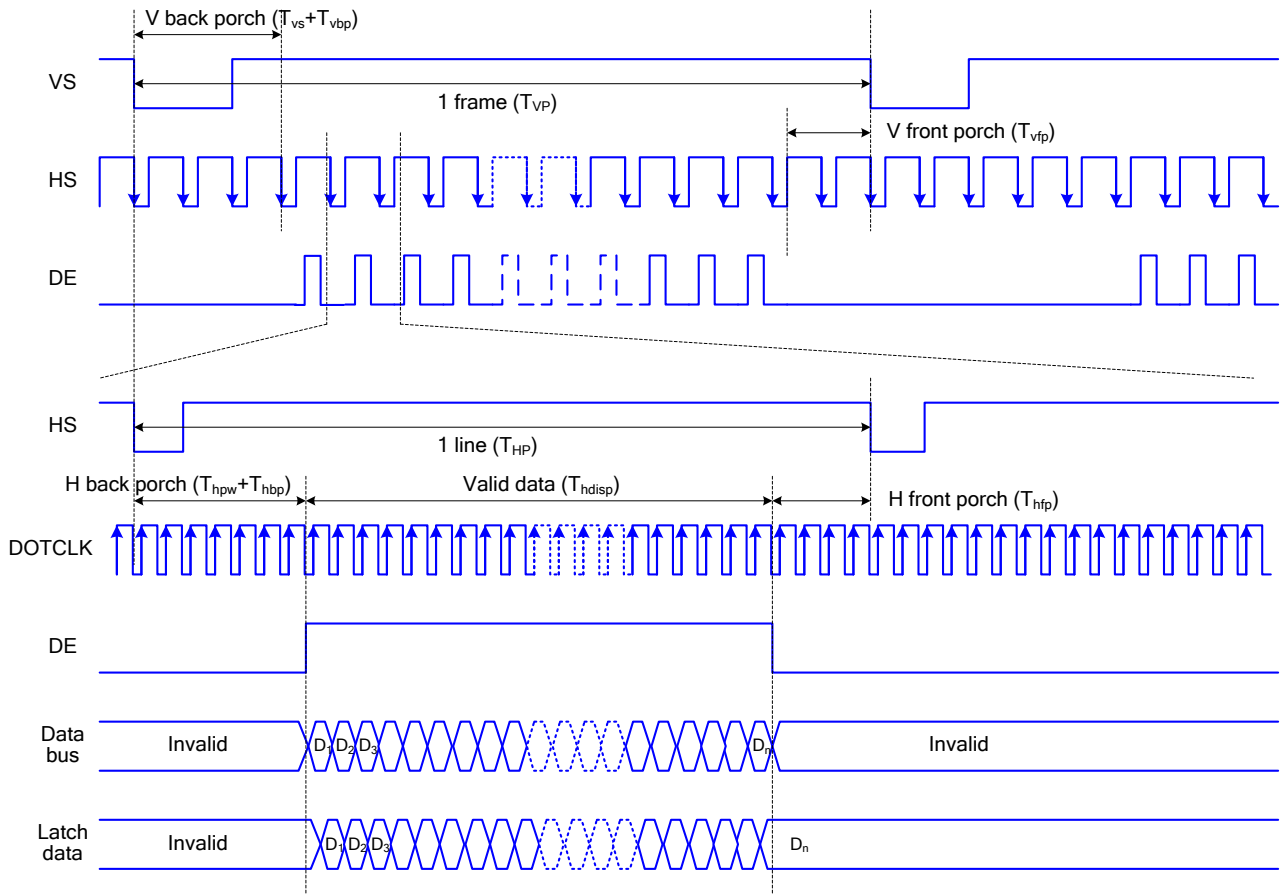
8.9.4 RGB Interface Mode Selection

ST77916 supports two kinds of RGB interface, DE mode and HV mode. Each mode also can select with ram and without ram. The table shown below uses command BDh, DB[7] to select with ram and without ram.

RCM	RGB Mode	WO	Data Path
0	DE mode	0	Ram
		1	Shift register (without Ram)
1	HV mode	0	Ram
		1	Shift register (without Ram)

8.9.5 RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Figure 25 Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.

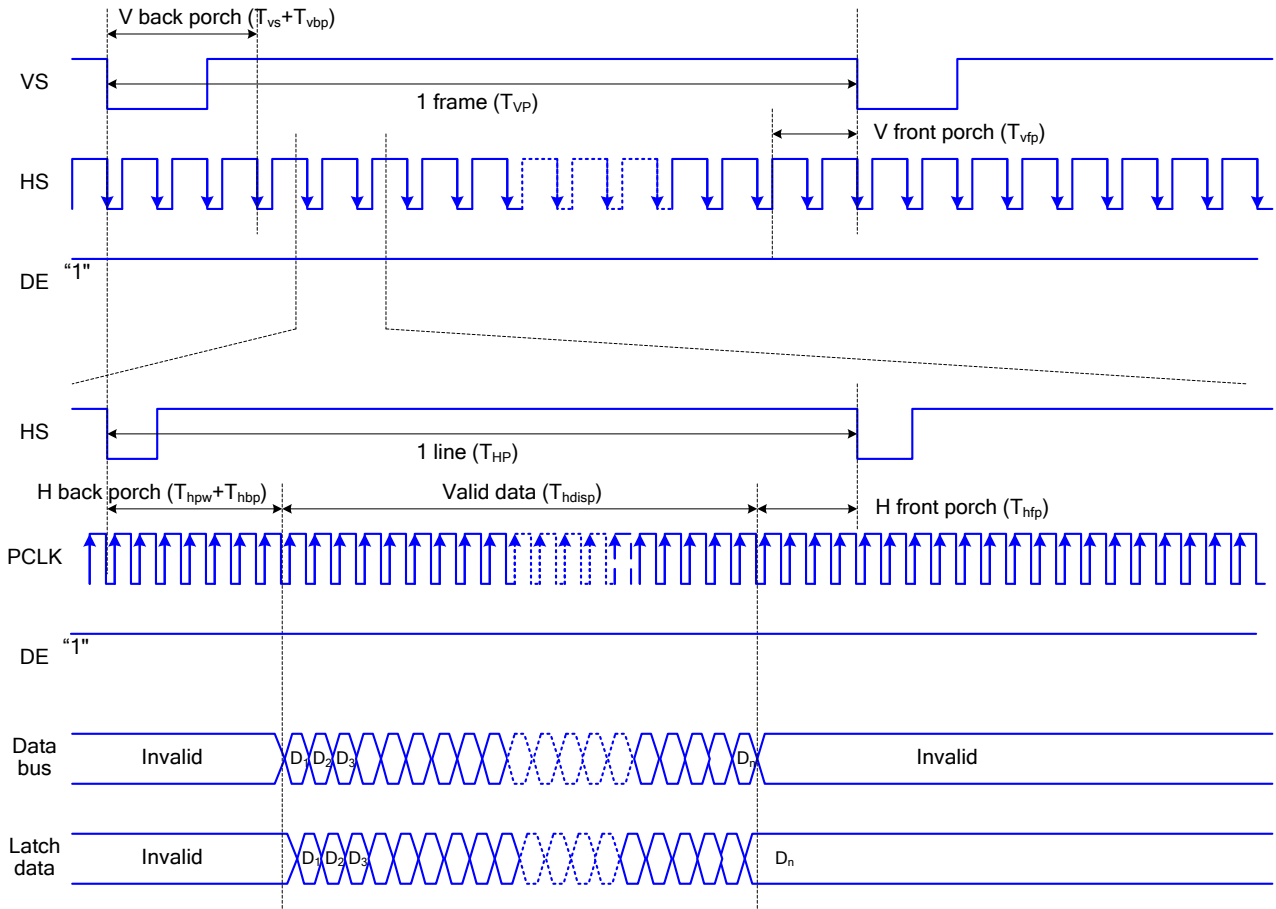


Figure 26 Timing chart of RGB interface HV mod

The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period.

In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

In 6-bit RGB interface mode, each of RGB dots are transferred in synchronization with DOTCLK signals. In other words, one pixel data needs to take three DOTCLKs to transfer.

In 6-bit RGB interface mode, the cycles of VSYNC, HSYNC, ENABLE, DOTCLK signals must be set correctly so that the data transfer is completed in units of pixels.

When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

In RGB interface mode, a RAM address is set in the address counter every frame on the falling edge of VSYNC.

8.10 Mobile Industry Processor Interface (MIPI)

8.10.1 Display Serial Interface (DSI)

1.1.1.1 GENAL DESCRIPTION

The communication can be separated 2 different levels between the MCU and the display module:

1. Low level communication what is done on the interface level
2. High level communication what is done on the packet level

1.1.1.2 Interface Level Communication

The display module uses data and clock lane differential pairs for DSI (DSI-1M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode. There are used different modes and protocols in each mode when there wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	CLOCK_P	CLOCK_N
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark – 0
LP-10	High (LP)	Low (LP)	Not Defined	LP – Request	Mark – 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes:

(1) Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

(2) If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

1.1.1.3 DSI-CLOCK Lanes

DSI-CLOCK_P/N lanes can be driven into three different power modes:

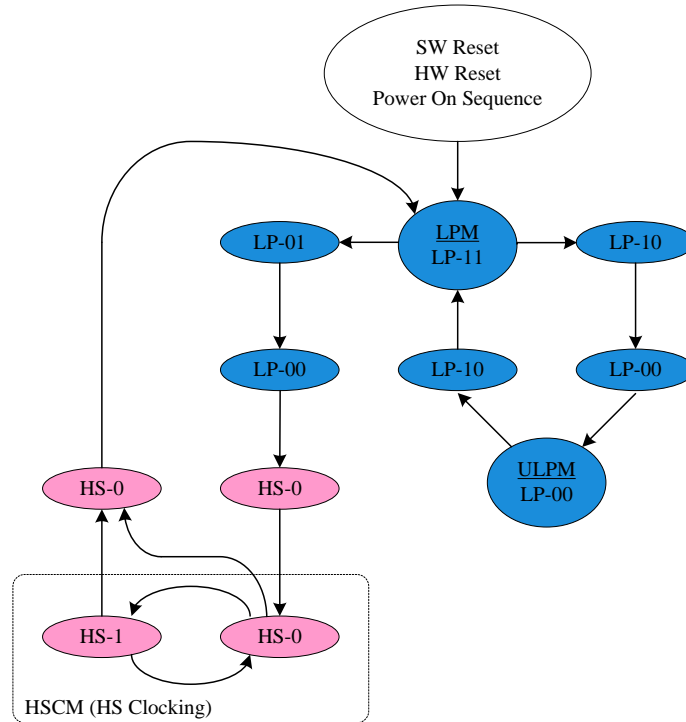
- ◆ Low Power Mode (LPM)
- ◆ Ultra Low Power Mode (ULPM)
- ◆ High Speed Clock Mode (HSCM)

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power

Mode (LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM). These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

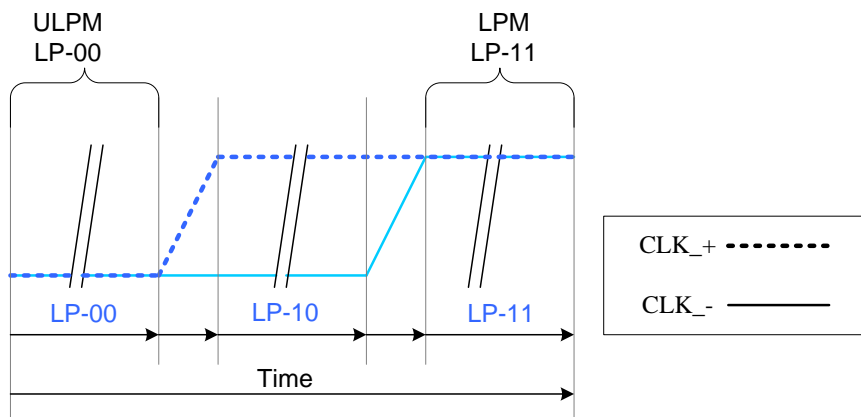


Flow chart of the different clock lanes

1. Low Power Mode (LPM)

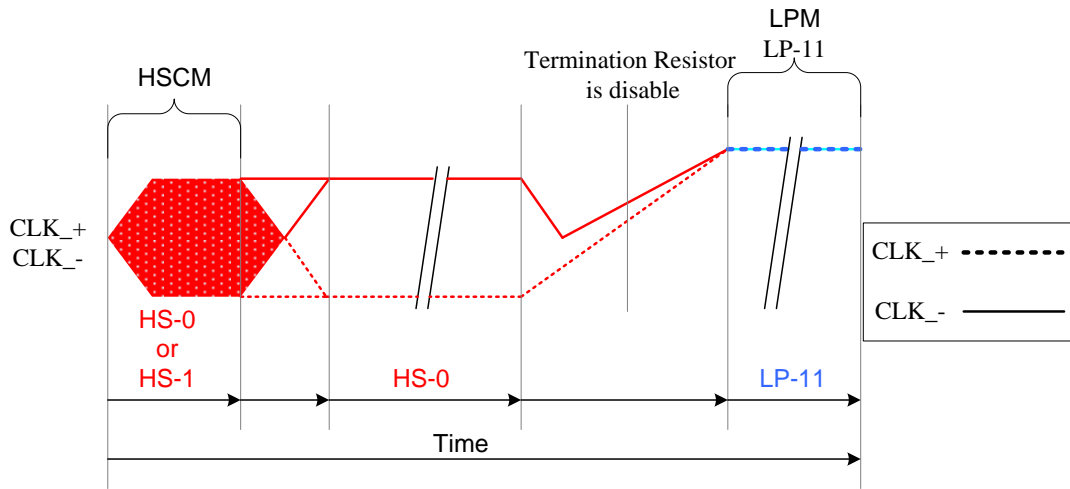
DSI-CLOCK_P/N lanes can be driven to the Low Power Mode (LPM), when DSI-CLOCK lanes are entering LP-11 State Code, in three different ways:

- ◆ After SW Reset, HW Reset or Power On Sequence =>LP-11 After DSI-CLOCK_P/N lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10
- ◆ LP-11 (LPM). This sequence is illustrated below.



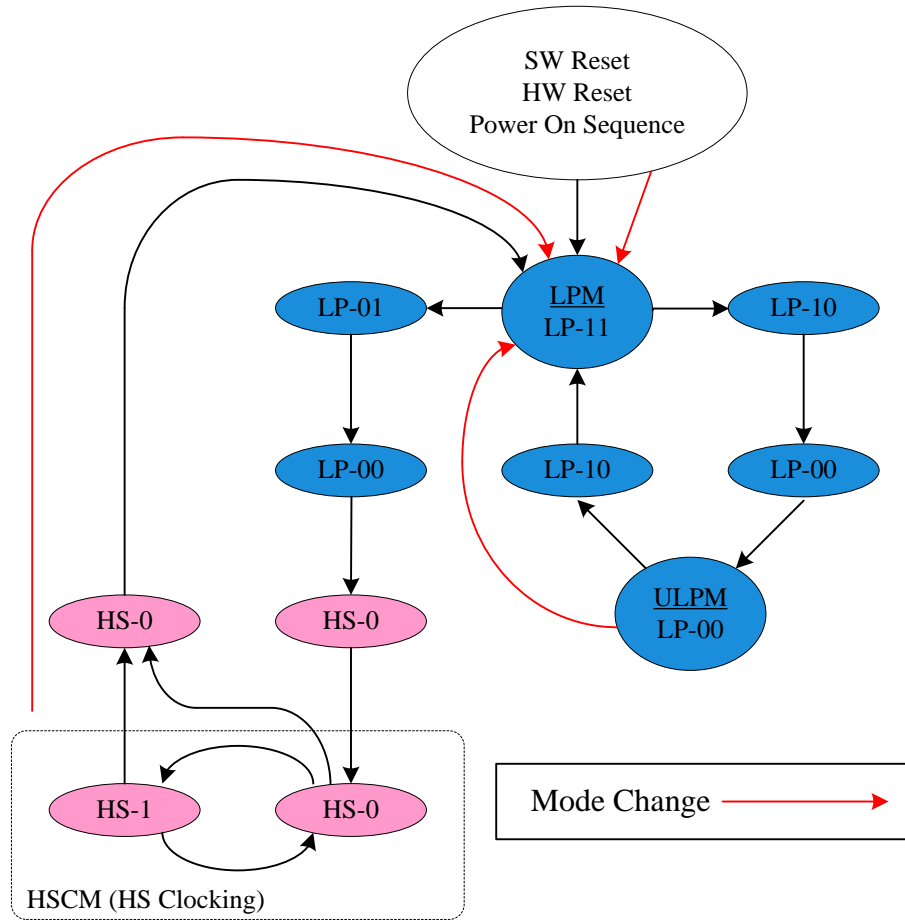
From ULPM to LPM

- ◆ After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0=>LP-11 (LPM). This sequence is illustrated below.



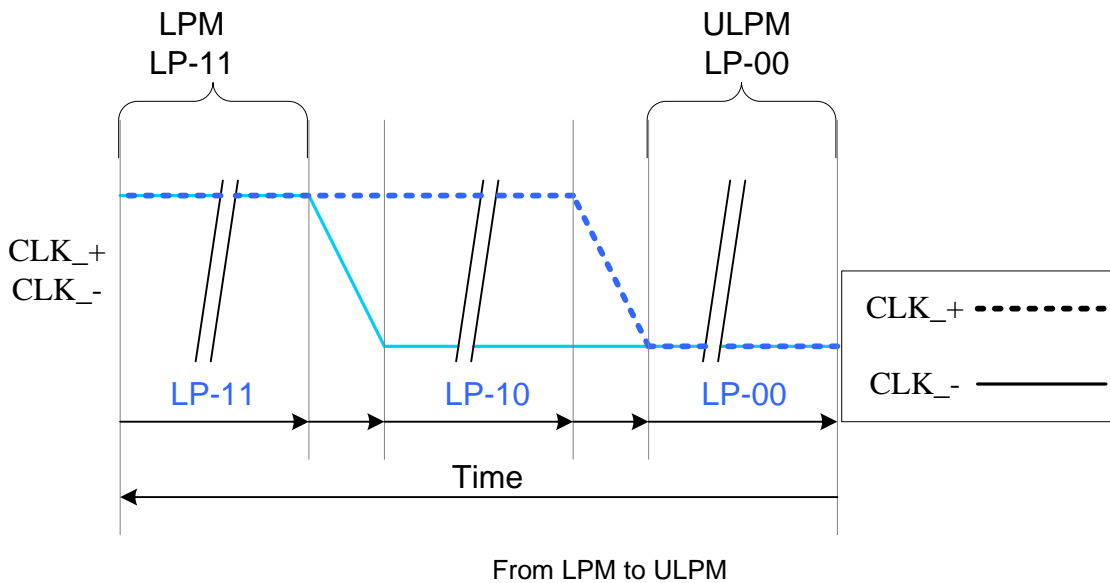
From High Speed Clock Mode (HSCM) to LPM

All three mode changes are illustrated a flow chart below.

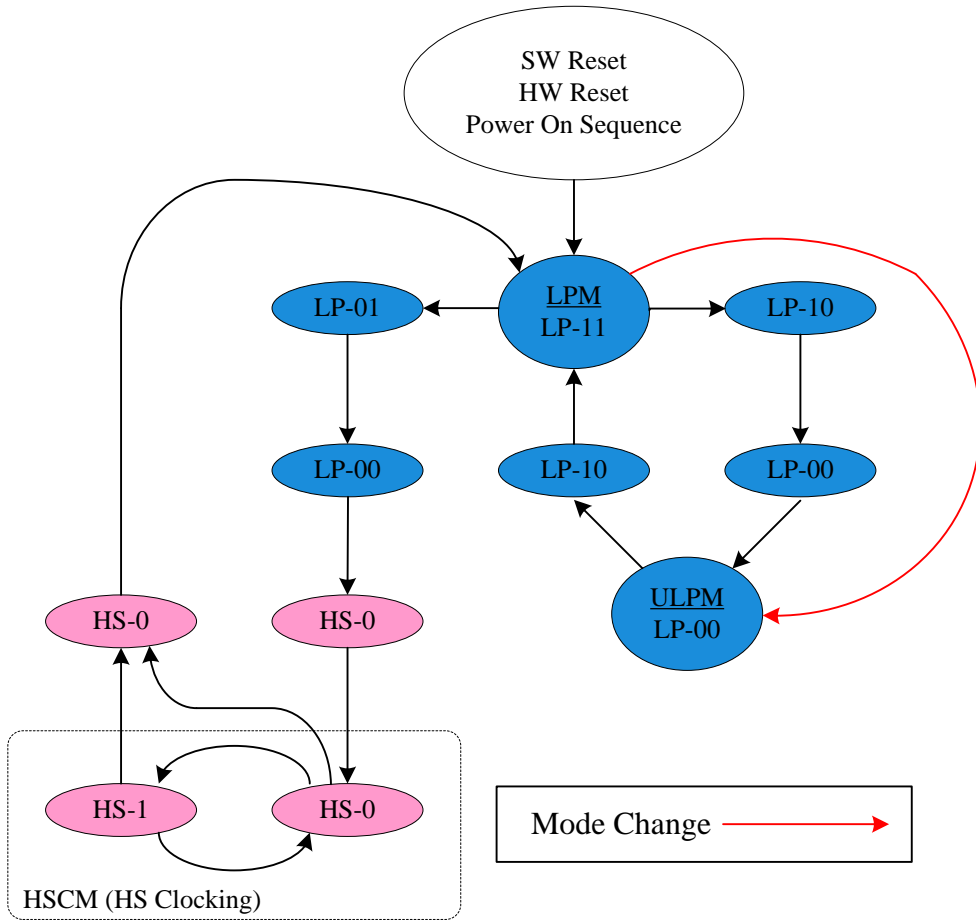


All Three Mode Changes to LPM on the Flow Chart

2. Ultra Low Power Mode (ULPM)

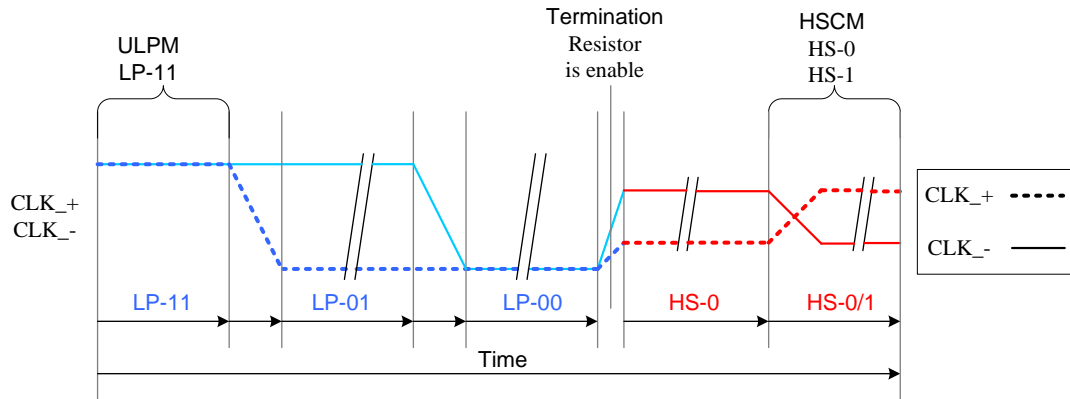


The mode change is also illustrated below.



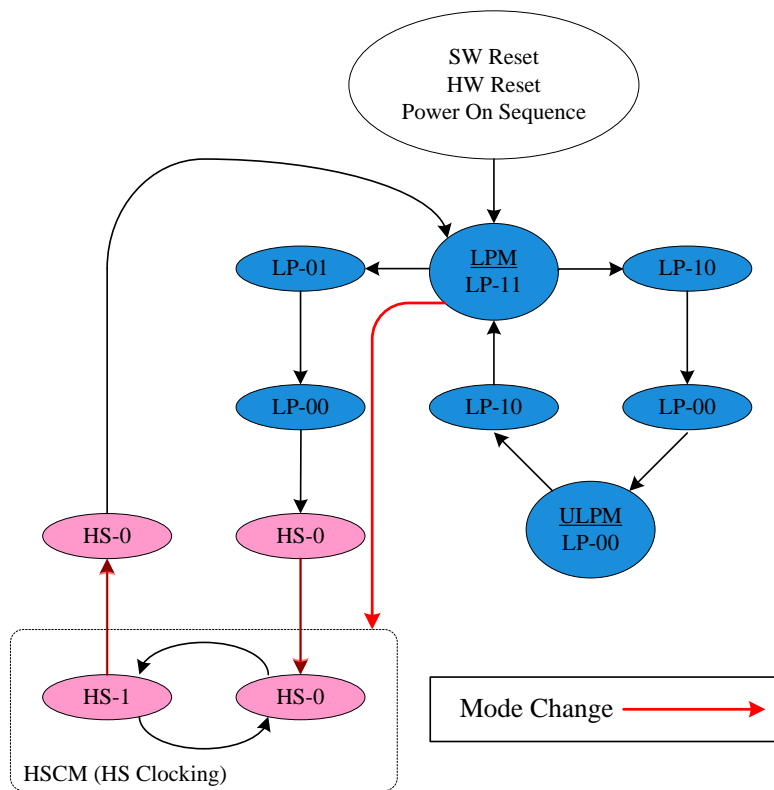
Mode Change from LPM to ULPM on the Flow Chart

3. High Speed Clock Mode (HSCM)



From LPM to HSCM

The mode change is also illustrated below.

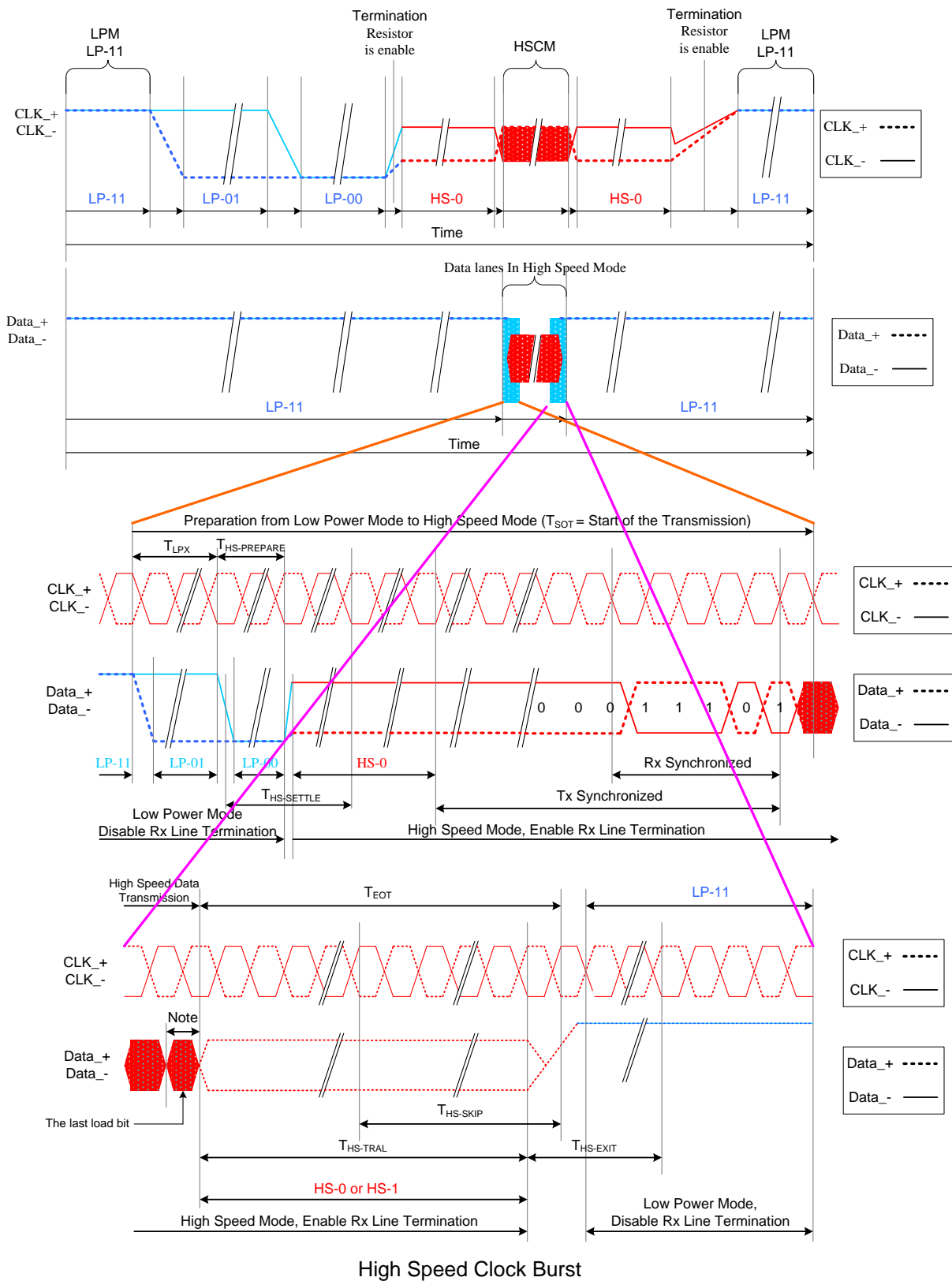


Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLOCK_P/N) is started before high speed data is sent via DSI-DATA_P/N lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0



Note:

If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0

1.1.1.4 DSI-DATA Lanes

DSI-DATA_P/N Data Lanes can be driven in different modes which are:

- ◆ Escape Mode
- ◆ High-Speed Data Transmission
- ◆ Bus Turnaround Request

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP-11(Mark-1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z, Note

1. Escape Mode

Data lanes (DSI-DATA_P/N) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

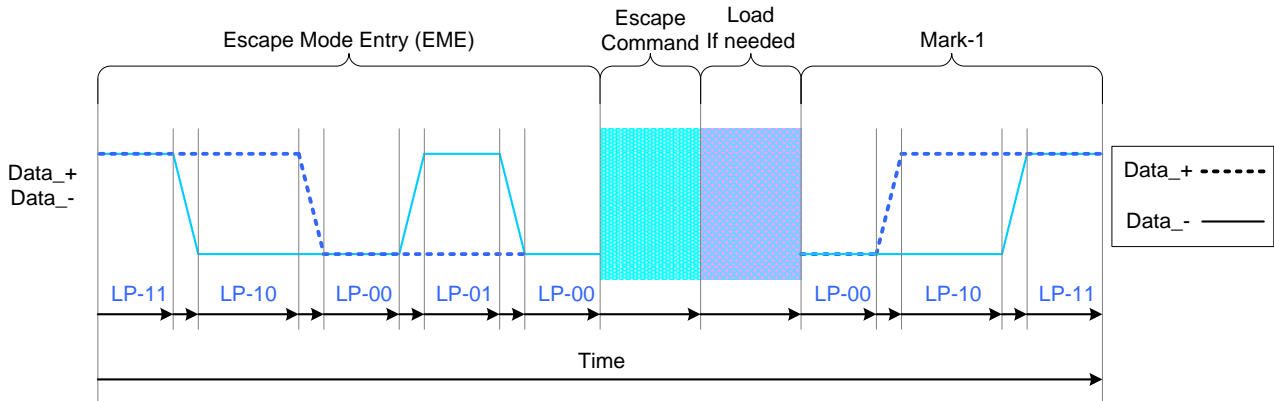
These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is reset the display module
- Indicate “Tearing Effect”, which is used for a TE line event from the display module to the MCU
- Indicate (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:



General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different Escape Commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (RX_D0P/N) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module an event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Escape commands are defined on the next table.

Escape command	Command Type Mode / Trigger	Entry command Pattern (First Last Bit Transmitted)
Low-Power Data	Mode	1110 0001 b
Ultra-Low Power Mode	Mode	0001 1110 b
Undefined-1, Note	Mode	1001 1111 b
Undefined-2, Note	Mode	1101 1110 b
Remote Application Reset	Trigger	0110 0010 b
Tearing Effect	Trigger	0101 1101 b
Acknowledge	Trigger	0010 0001 b
Uknown-5, Note	Trigger	1010 0000 b

Note: This Escape command support has not been implemented on the display module.

Low-Power Data Transmission (LPDT)

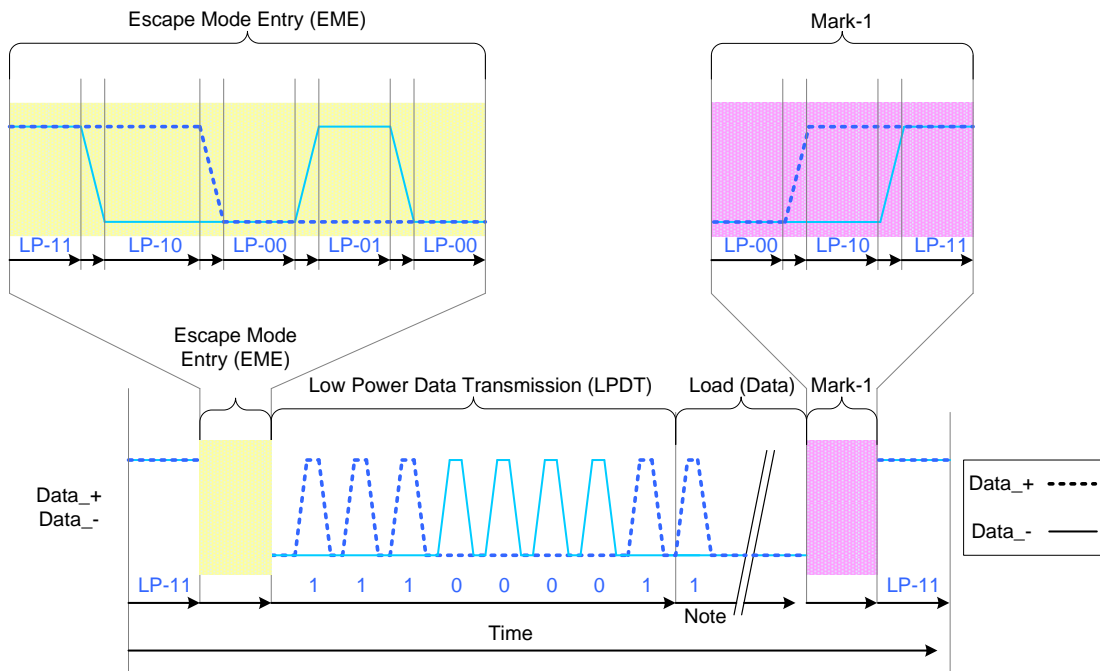
The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11

- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):
One or more bytes (8 bit)
Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

The Low-Power Data Transmission (LPDT) is as below,



Note : Load (Data) is presenting that the first bit is logical "1" in this Exsample

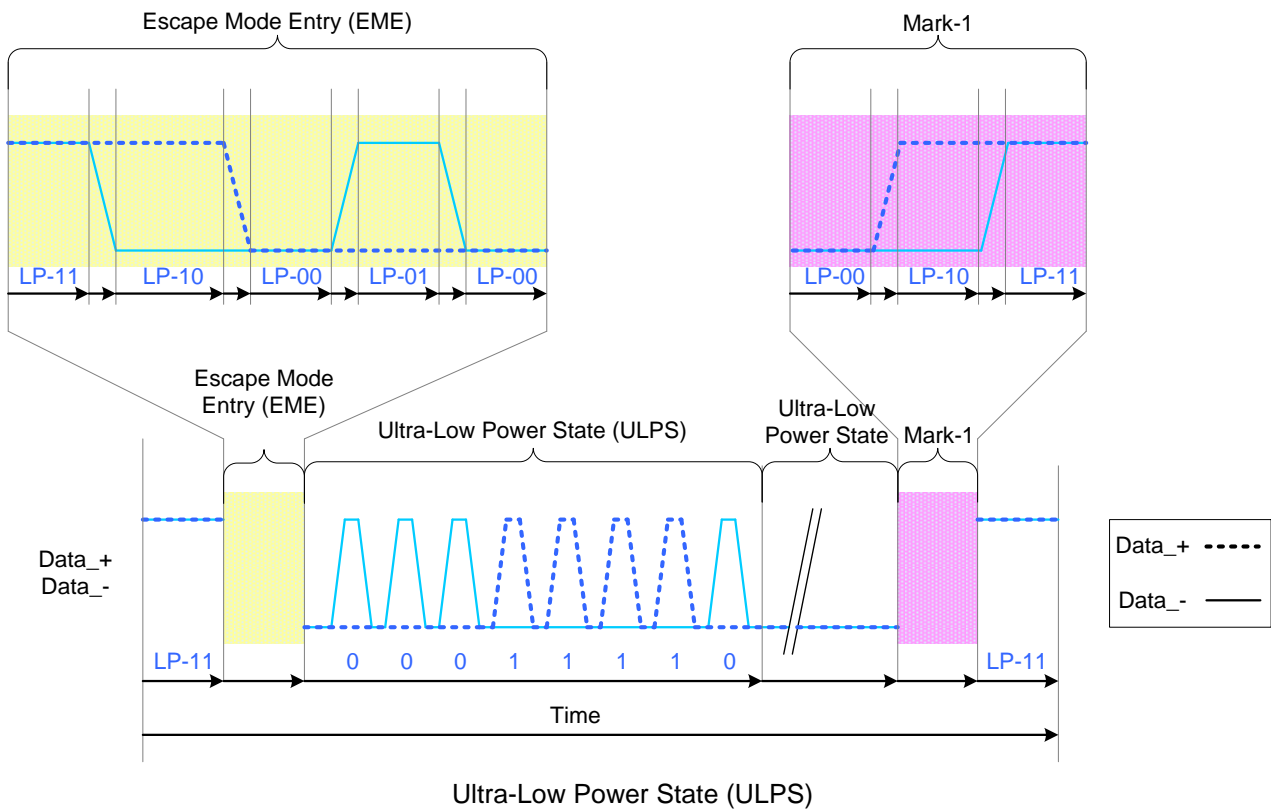
Low-Power Data Transmission (LPDT)

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode. The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



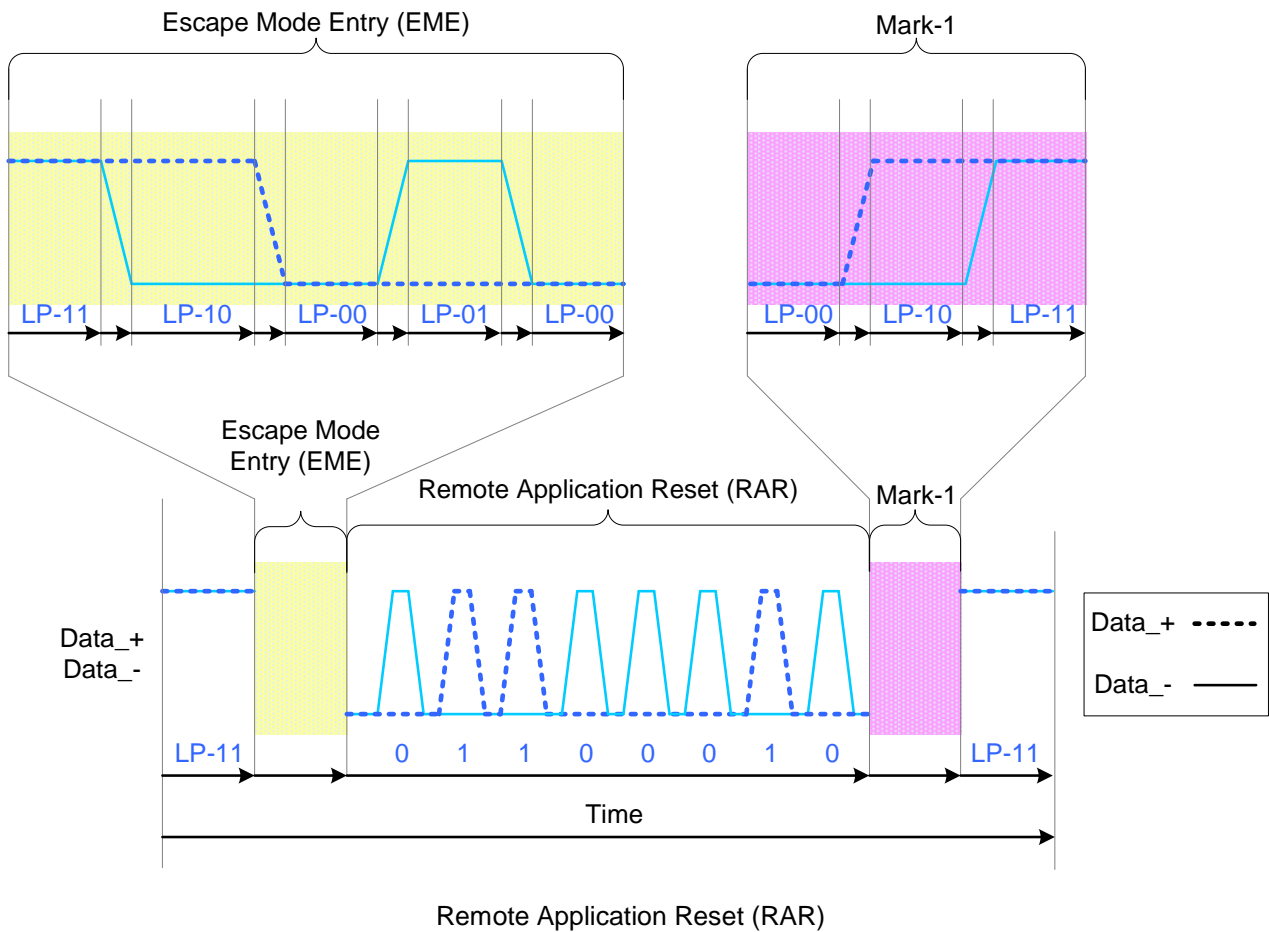
Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Remote Application Reset (RAR)

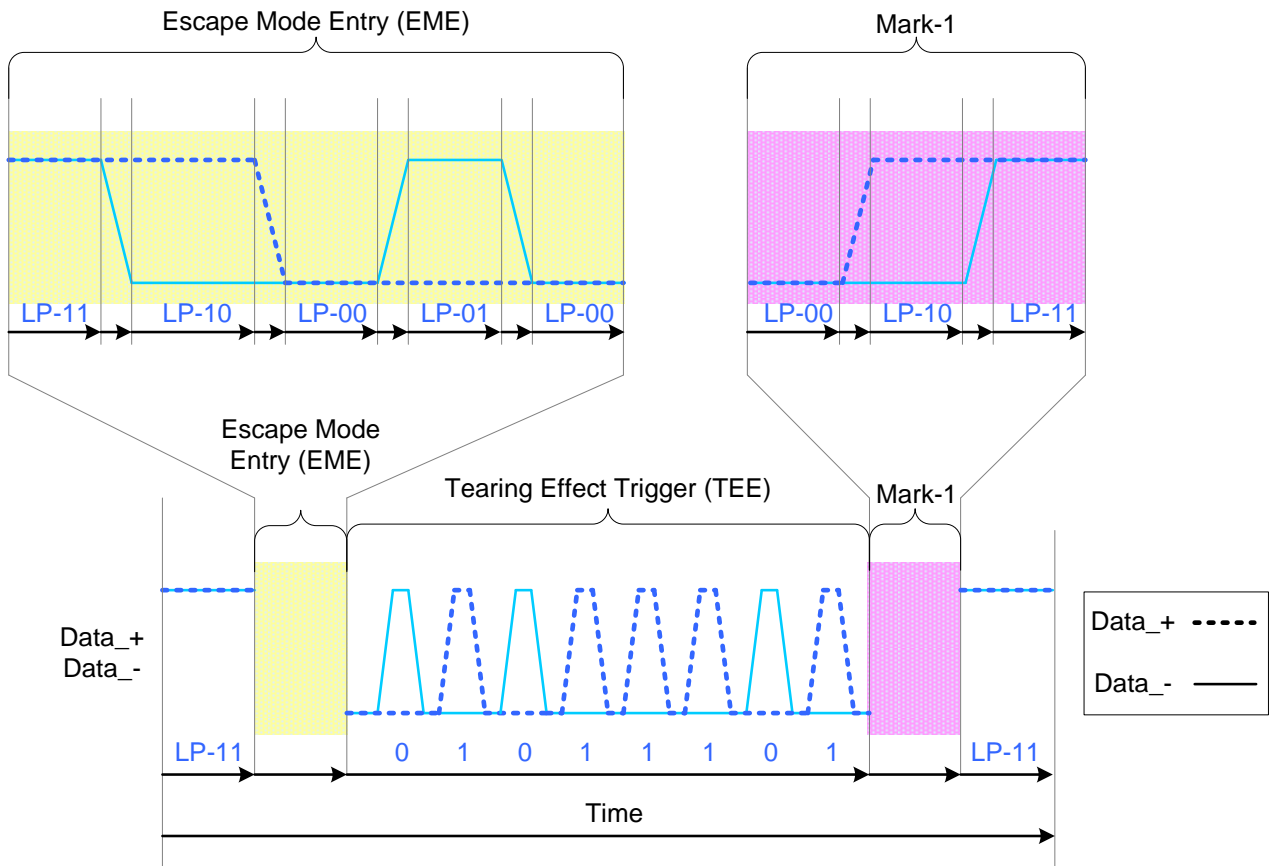
Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happened on the display module by Tearing Effect (TEE).

The display module is sending the Tearing Effect (TEE) what is a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Tearing Effect (TEE)

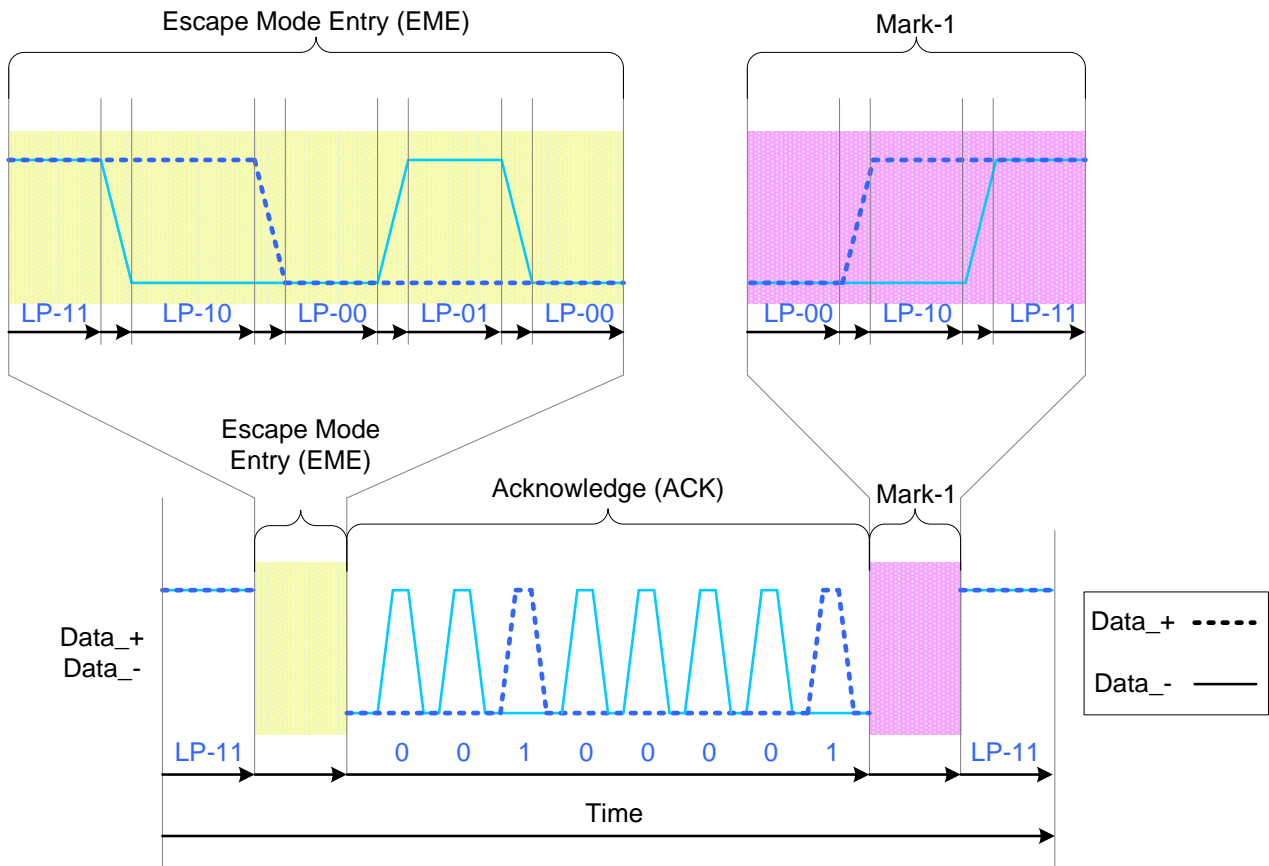
Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The display module is sending the Acknowledge (ACK) what is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Acknowledge (ACK)

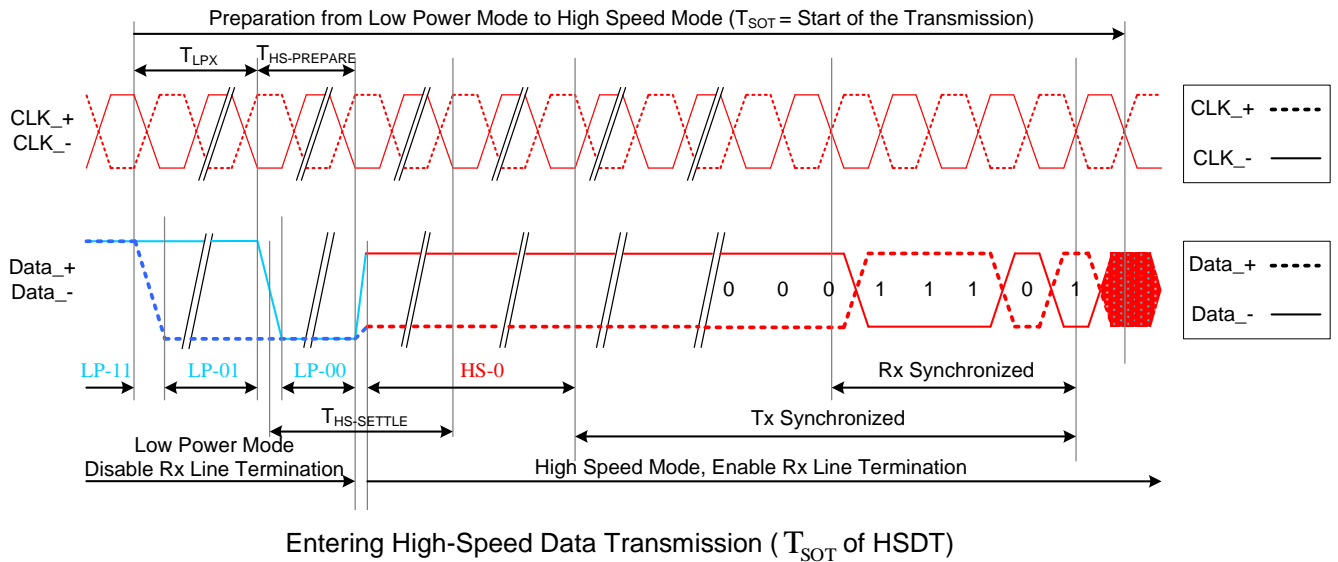
2. High-Speed Data Transmission

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes RX_CP/N have already been entered in the High-Speed Clock Mode (HSCM) by the MCU.

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below



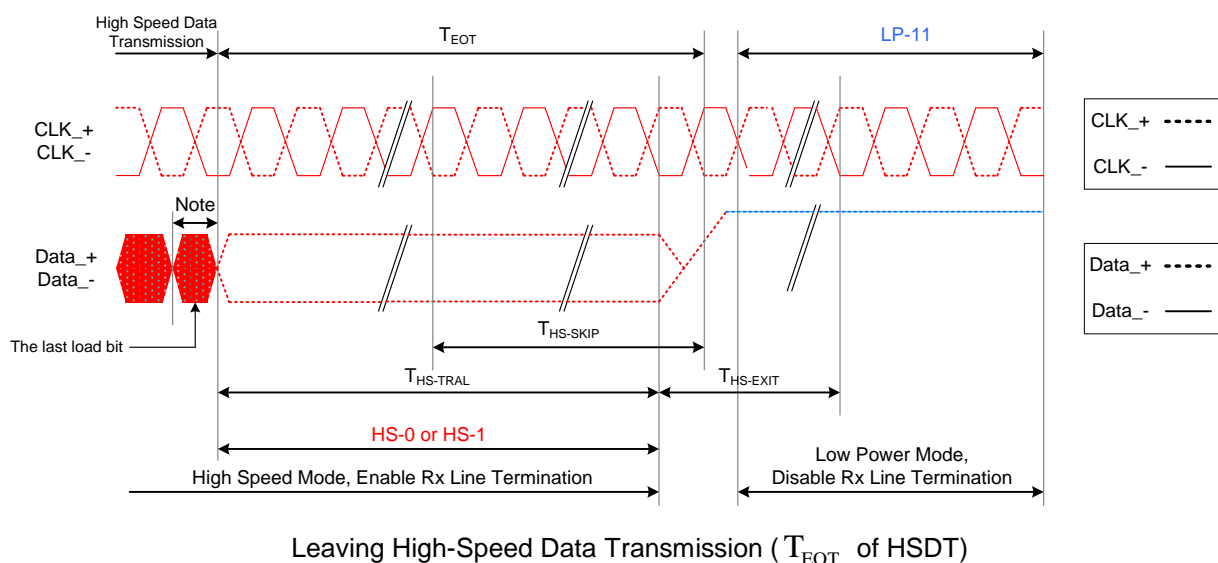
Leaving High-Speed Data Transmission

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes RX_CP/N are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode.

Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
 - MCU changes to HS-1, if the last load bit is HS-0
 - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

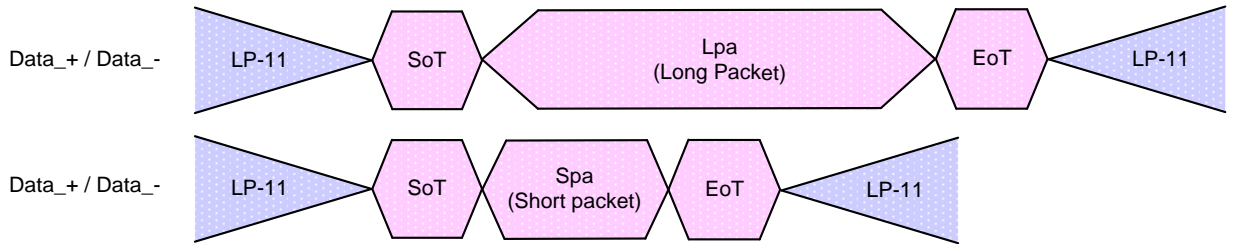
This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below



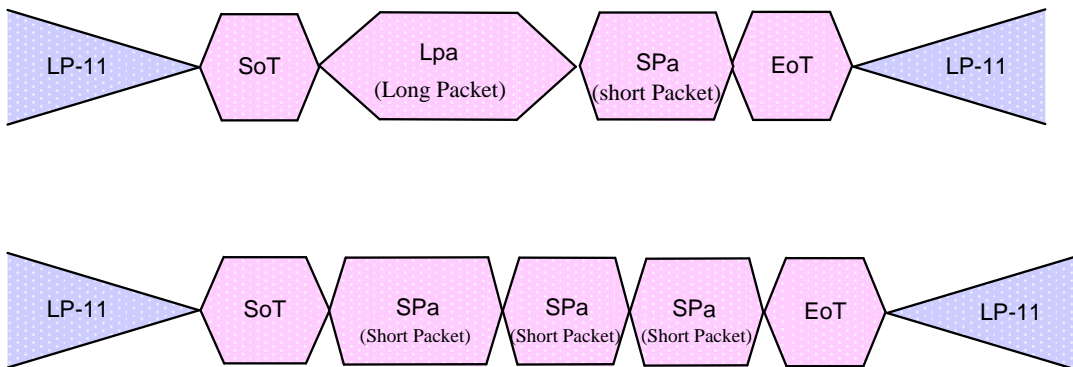
Burst of the High-Speed Data Transmission

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (Lpa) or Short (Spa) packets.

The single packet in High-Speed Data Transmission is illustrated for reference purposes below:

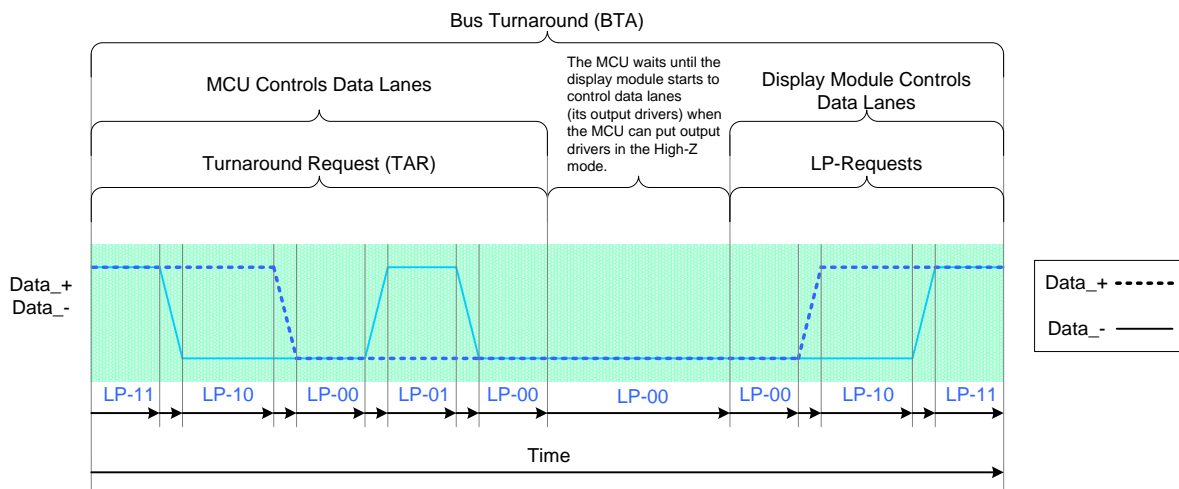


The multiple packets in High-Speed Data Transmission is illustrated for reference purposes below:



3. Bus Turnaround Request

The MCU which is controlling DSI-DATA_P/N Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or Display Module. The MCU and Display Module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to Display Module, as follows.

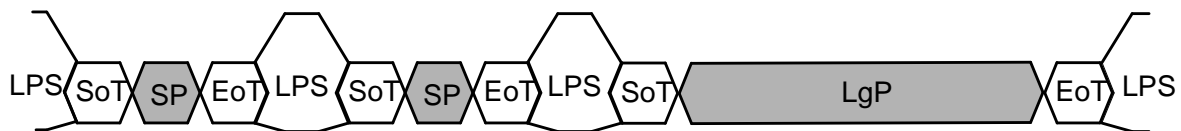


8.10.2 DSI protocol

The Protocol layer appends packet-protocol information and headers, and then sends complete bytes through the Lane Management layer to the PHY. Packets are serialized by the PHY and sent across the serial Link. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands.

1.1.1.5 Multiple Packets per Transmission

There are two modes of data transmission, HS and LP transmission modes, at the PHY layer. Before a HS transmission can be started, the transmitter PHY issues a SoT sequence to the receiver. After that, data or command packets can be transmitted in HS mode. Multiple packets may exist within a single HS transmission and the end of transmission is always signaled at the PHY layer using a dedicated EoT sequence. In order to enhance the overall robustness of the system, DSI defines a dedicated EoT packet (EoTp) at the protocol layer for signaling the end of HS transmission. For backwards compatibility with earlier DSI systems, the capability of generating and interpreting this EoTp can be enabled or disabled.



Separate Transmissions

Key:

LPS -- Low power state SP -- Short Packet
 SoT -- Start of Transmission LgP -- Long Packet
 EoT -- End of Transmission



Single Transmissions

1.1.1.6 Packet Composition

The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. For example, in Video Mode systems in a display application the logical unit for a packet may be one horizontal display line. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

Packet sizes fall into two categories:

- **Short packets** are four bytes in length including the ECC. Short packets are used for most Command Mode commands and associated parameters. Other Short packets convey events like H Sync and V Sync edges. Because they are Short packets they can convey accurate timing information to logic at the peripheral.
- **Long packets** specify the payload length using a two-byte Word Count field. Payloads may be

from 0 to $2^{16}-1$ bytes long. Therefore, a Long packet may be up to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.

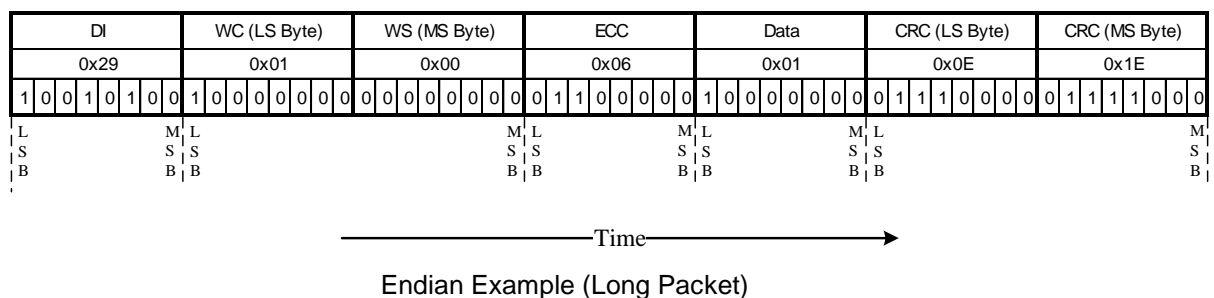
A special case of Command Mode operation is video-rate (update) streaming, which takes the form of an arbitrarily long stream of pixel or other data transmitted to the peripheral. As all DSI transactions use packets, the video stream shall be broken into separate packets. This “packetization” may be done by hardware or software. The peripheral may then reassemble the packets into a continuous video stream for display.

The Set Maximum Return Packet Size command allows the host processor to limit the size of response packets coming from a peripheral.

1.1.1.7 Endian Policy

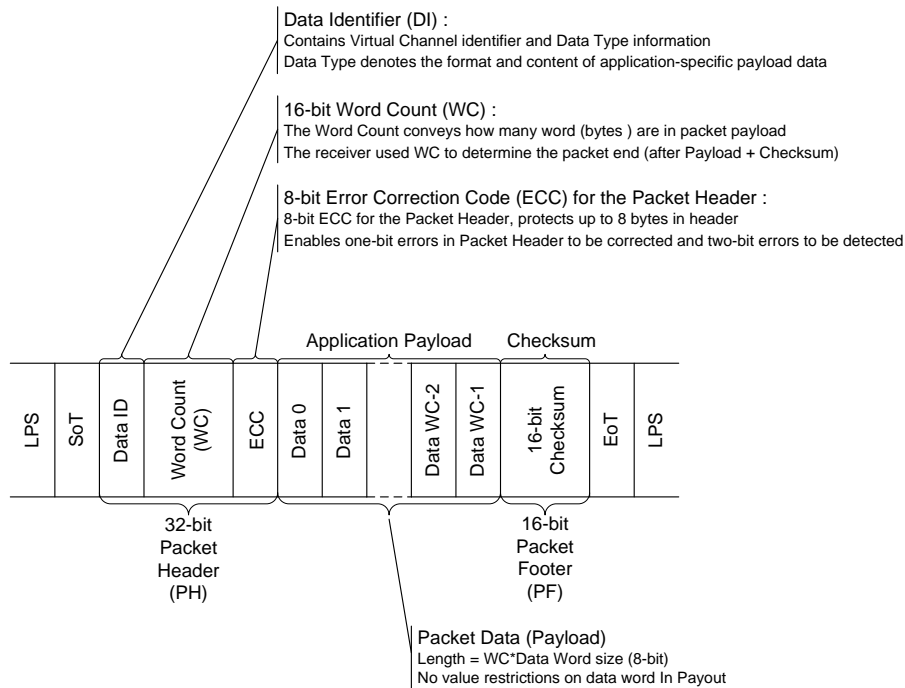
All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

Figure 12 shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.



1.1.1.8 General Packet Structure (Long Packet Format)

A Long packet shall consist of three elements: a 32-bit Packet Header (PH), an application-specific Data Payload with a variable number of bytes, and a 16-bit Packet Footer (PF). The Packet Header is further composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.



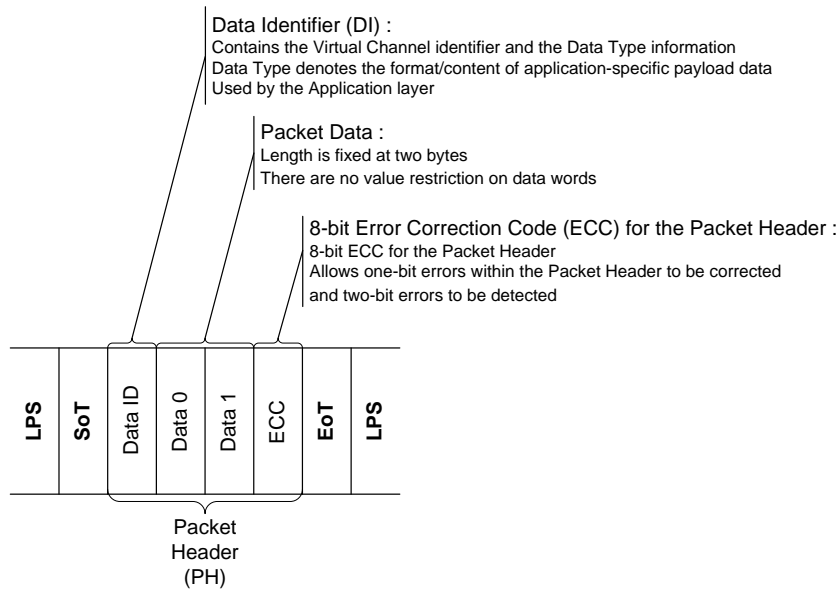
Long Packet Structure

The Data Identifier defines the Virtual Channel for the data and the Data Type for the application specific payload data. See sections 8.8 through 8.10 for descriptions of Data Types. The Word Count defines the number of bytes in the Data Payload between the end of the Packet Header and the start of the Packet Footer. Neither the Packet Header nor the Packet Footer shall be included in the Word Count. The Error Correction Code (ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. This includes both the Data Identifier and Word Count fields. After the end of the Packet Header, the receiver reads the next Word Count * bytes of the Data Payload. Within the Data Payload block, there are no limitations on the value of a data word, i.e. no embedded codes are used. Once the receiver has read the Data Payload it reads the Checksum in the Packet Footer. The host processor shall always calculate and transmit a Checksum in the Packet Footer. Peripherals are not required to calculate a Checksum. Also note the special case of zero-byte Data Payload: if the payload has length 0, then the Checksum calculation results in (FFFFh). If the Checksum is not calculated, the Packet Footer shall consist of two bytes of all zeros (0000h). See section 9 for more information on calculating the Checksum. In the generic case, the length of the Data Payload shall be a multiple of bytes. In addition, each data format may impose additional restrictions on the length of the payload data, e.g. multiple of four bytes. Each byte shall be transmitted least significant bit first. Payload data may be transmitted in any byte order restricted only by data format requirements. Multi-byte elements such as Word Count and Checksum shall be transmitted least significant byte first

1.1.1.9 General Packet Structure (Short Packet Format)

A Short packet shall contain an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC; a Packet Footer shall not be present. Short packets shall be four bytes in length. The Error Correction Code

(ECC) byte allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.



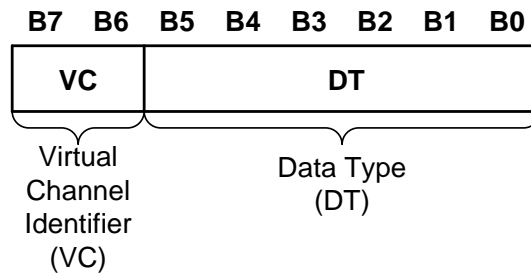
Short Packet Structure

1.1.1.10 Common Packet Elements

Long and Short packets have several common elements that are described in this section.

➤Data Identifier Byte

The first byte of any packet is the DI (Data Identifier) byte. Figure 15 shows the composition of the Data Identifier (DI) byte. DI[7:6]: These two bits identify the data as directed to one of four virtual channels. DI[5:0]: These six bits specify the Data Type.

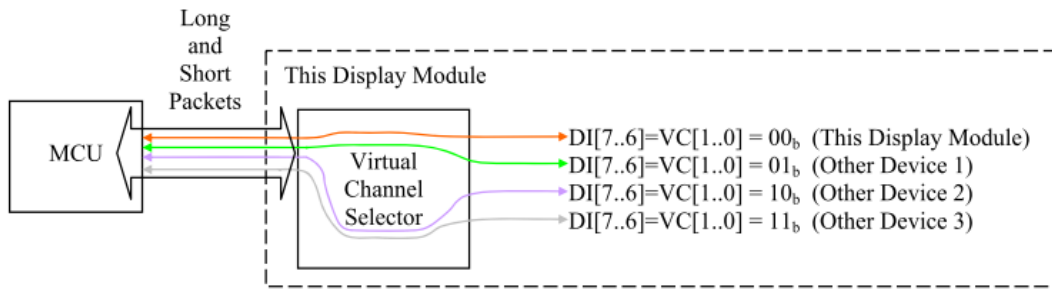


Data Identifier Byte

Virtual Channel Identifier – VC field, DI[7:6]

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel. Note that packets sent in a single transmission each have their own Virtual Channel assignment and can be directed to different peripherals. Although the DSI protocol permits communication with multiple peripherals, this specification only addresses the connection of a host processor to a single peripheral. Implementation details for connection to more than one physical peripheral are beyond the scope

of this document.



Virtual Channel (VC) Configuration

Data Type Field DT[5:0]

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start / end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet. When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

1.1.1.11 Error Correction Code

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte. Peripherals shall support ECC in both forward- and reverse-direction communications.

Bits (P[7...0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

$$\begin{aligned}
 P7 &= 0 \\
 P6 &= 0 \\
 P5 &= D10 \wedge D11 \wedge D12 \wedge D13 \wedge D14 \wedge D15 \wedge D16 \wedge D17 \wedge D18 \wedge D19 \wedge D21 \wedge D22 \wedge D23 \\
 P4 &= D4 \wedge D5 \wedge D6 \wedge D7 \wedge D8 \wedge D9 \wedge D16 \wedge D17 \wedge D18 \wedge D19 \wedge D20 \wedge D22 \wedge D23 \\
 P3 &= D1 \wedge D2 \wedge D3 \wedge D7 \wedge D8 \wedge D9 \wedge D13 \wedge D14 \wedge D15 \wedge D19 \wedge D20 \wedge D21 \wedge D23 \\
 P2 &= D0 \wedge D2 \wedge D3 \wedge D5 \wedge D6 \wedge D9 \wedge D11 \wedge D12 \wedge D15 \wedge D18 \wedge D20 \wedge D21 \wedge D22 \\
 P1 &= D0 \wedge D1 \wedge D3 \wedge D4 \wedge D6 \wedge D8 \wedge D10 \wedge D12 \wedge D14 \wedge D17 \wedge D20 \wedge D21 \wedge D22 \wedge D23 \\
 P0 &= D0 \wedge D1 \wedge D2 \wedge D4 \wedge D5 \wedge D7 \wedge D10 \wedge D11 \wedge D13 \wedge D16 \wedge D20 \wedge D21 \wedge D22 \wedge D23
 \end{aligned}$$

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63...0]), but this implementation is based on 24 bit value (D [23...0]). Therefore, there is only needed 6 bits (P [5...0]) for Error Correction Code (ECC).

DI								Data0								Data1								ECC							
0x05								0x10								0x00								0x2C							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
D	D	D		D	D		D		D	D		D				D				D	D	D	D	P							
0	1	2		4	5		7		10	11		13				16				20	21	22	23	0							
D	D		D	D		D		D	D		D				D				D	D	D	D		P							
0	1		3	4		6		8	10	12		14			17				20	21	22	23		1							
D		D	D		D	D		D	D	D		D			D				D	D	D	D			P						
0		2	3		5	6		9	11	12		15			18				20	21	22				2						
	D	D	D						D	D	D					D	D	D		D	D	D				P					
	1	2	3					7	8	9					19	20	21		23							3					
				D	D	D	D								D	D	D	D	D	D	D	D					P				
				4	5	6	7	8	9						16	17	18	19	20		22	23					4				
																												P			
																												5			
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
L								M	L						M	L							M	L							
S								S	S						S	S							S	S							
B								B	B						B	B							B	B							

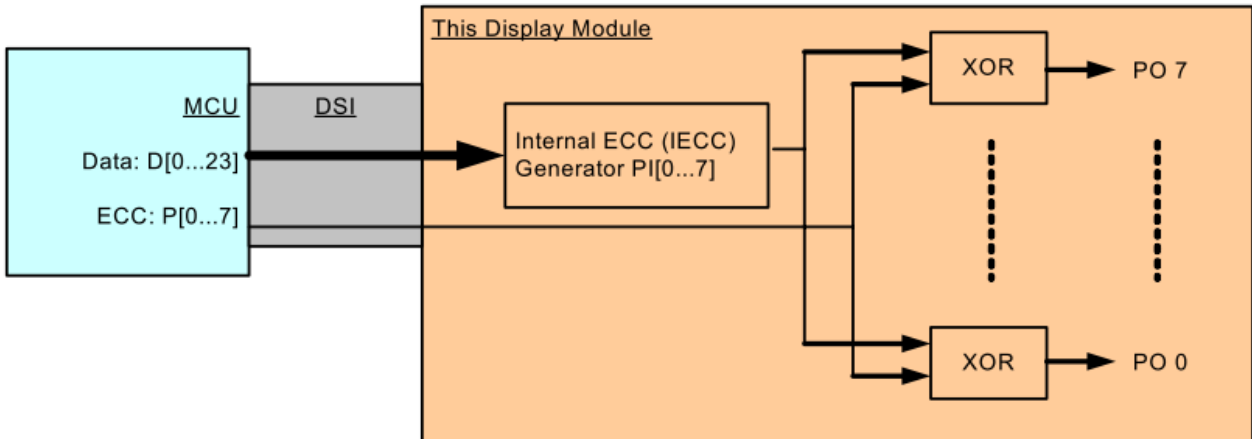
XOR Functionality on the Short Packet (Spa)

DI								WC (LS Byte)								WC (MS Byte)								ECC							
0x29								0x01								0x00								0x06							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
D	D	D		D	D		D		D	D		D				D				D	D	D	D	P							
0	1	2		4	5		7		10	11		13				16				20	21	22	23	0							
D	D		D	D		D		D	D		D				D				D	D	D	D		P							
0	1		3	4		6		8	10	12		14			17				20	21	22	23		1							
D		D	D		D	D		D	D	D		D			D				D	D	D	D			P						
0		2	3		5	6		9	11	12		15			18				20	21	22				2						
	D	D	D						D	D	D					D	D	D		D	D	D				P					
	1	2	3					7	8	9					19	20	21		23							3					
				D	D	D	D								D	D	D	D	D	D	D	D					P				
				4	5	6	7	8	9						16	17	18	19	20		22	23					4				
																												P			
																												5			
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
L								M	L						M	L							M	L							
S								S	S						S	S							S	S							
B								B	B						B	B							B	B							

XOR Functionality on the Long Packet (Lpa)

The transmitter (The MCU or the Display Module) is sending data bits D[23:0] and Error Correction Code (ECC) P[7:0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction

Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7:0].



Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23:0]) and ECC (P[7:0]) are received correctly, if a value of the PO[7:0] is 00h.
 The sent data bits (D[23:0]) and ECC (P[7:0]) are not received correctly, if a value of the PO[7:0] is not 00h.

ECC P[7:0]	1 1 0 0 0 0 0 0	03h
IECC PI[7:0]	1 1 0 0 0 0 0 0	03h
XOR(ECC,IECC)	0 0 0 0 0 0 0 0	=00h => No Error
	L	M
	S	S
	B	B

Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7:0]	1 1 0 0 0 0 0 0	03h
IECC PI[7:0]	1 1 1 1 0 0 0 0	0Fh
XOR(ECC,IECC)	0 0 1 1 0 0 0 0	=0Ch => Error
	L	M
	S	S
	B	B

Internal XOR Calculation between ECC and IECC Values – Error

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

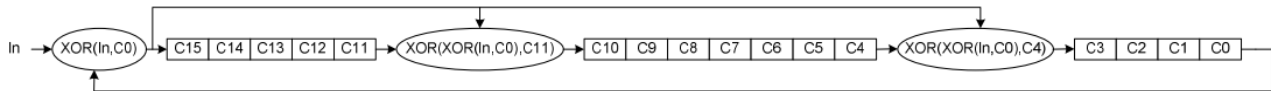
One error is detected if the value of the PO[7:0] is on the above table : One it Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO [7...0] = 0Eh
- The bit of the data (D [23:0]), what is not correct, is D[3]

More than one error is detected if the value of the PO [7...0] is not on the above table: One Bit Error Value of the Error Correction Code (ECC) e.g. PO [7...0] = 0Ch.

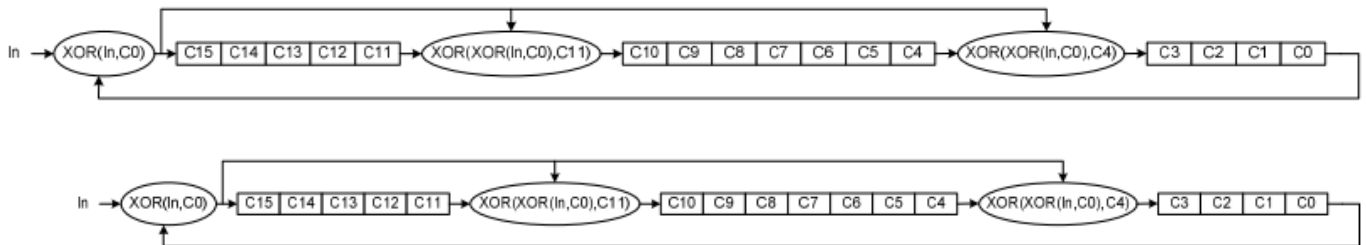
1.1.1.12 Packet Footer on the Long Packet

Packet Footer (PF) of the Long Packet (Lpa) is defined after the Packet Data (PD) of the Long Packet (Lpa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (Lpa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X_{16} + X_{12} + X_5 + X_0$ as it is illustrated below.



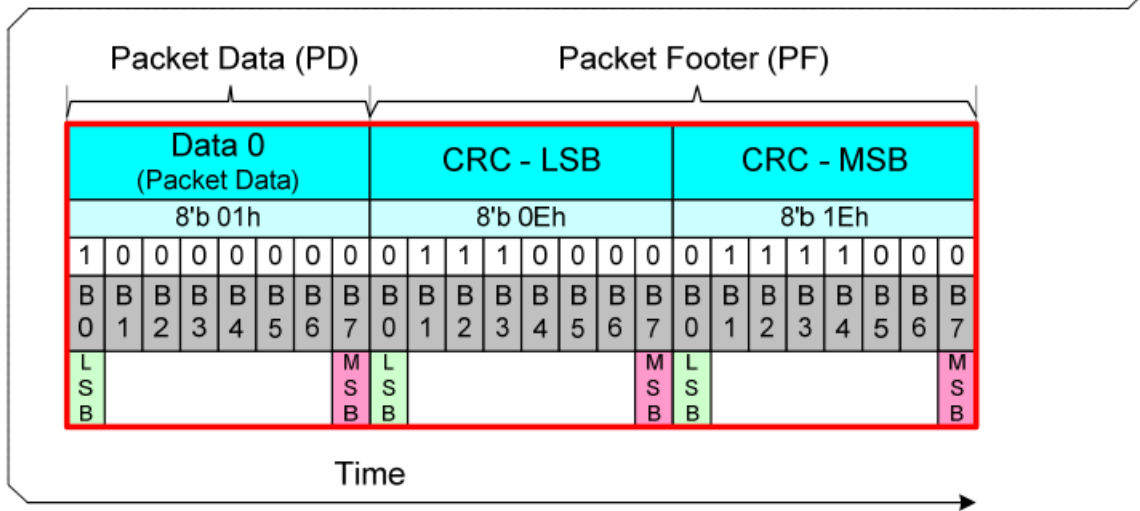
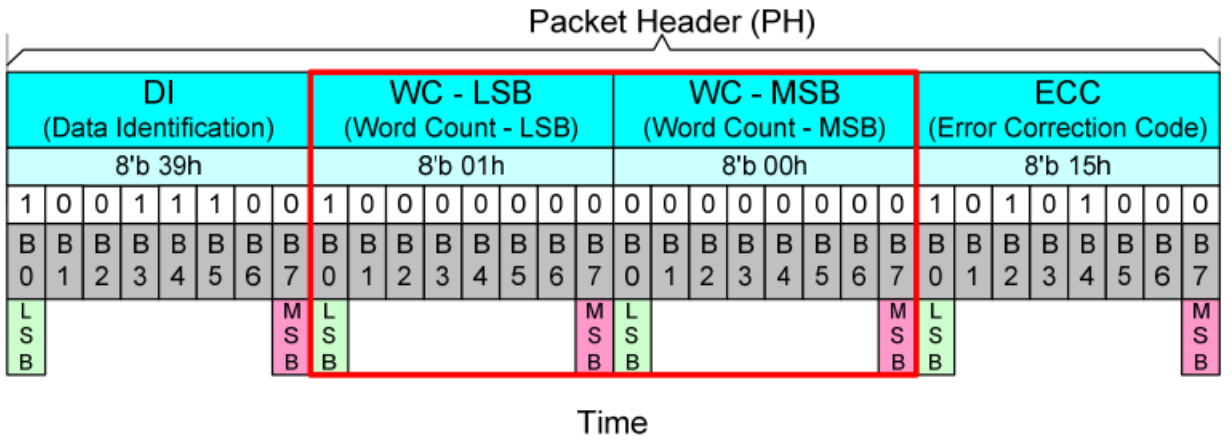
The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (Lpa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11)(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4)(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0			1	1	1	0	
			MSB																		LSB

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) is equal and vice versa the received Packet Data (PD) and Packet Footer(PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

1.1.1.13 Processor to Peripheral Direction Packet Data Types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are show as below table.

Data type	Data type, binary	Description packet	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
02h	00 0010	Color Mode (CM) Off Command	Short
12h	01 0010	Color Mode (CM) On Command	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter	Short
23h	10 0011	Generic Short WRITE, 2 parameters	Short
04h	00 0100	Generic READ, no parameters	Short
14h	01 0100	Generic READ, 1 parameter	Short
24h	10 0100	Generic READ, 2 parameters	Short
05h	00 0101	DCS Short WRITE, no parameters	Short
15h	01 0101	DCS Short WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h / XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	

Data Types for Processor-sourced Packets

All detail function of data types is as below :

Sync event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type, hex	Function description	Number of bytes
01h	Sync Event, V Sync Start	Short
11h	Sync Event, V Sync End	Short
21h	Sync Event, H Sync Start	Short
31h	Sync Event, H Sync End	Short
<p>Note: In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA.</p>		

Color mode status (Color Mode On, Color Mode Off)		
Data type, hex	Function description	Number of bytes
02h	Color Mode On that switches a Video Mode display module to a low-color mode for power saving.	Short
12h	Color Mode Off that switches a Video Mode display module from low-color display to normal display.	Short

Display status (shutdown command, turn-on command)		
Data type, hex	Function description	Number of bytes
22h	Shutdown Peripheral command that turns off the display in a Video Mode display for power saving.	Short
32h	Turn On Peripheral command that turns on the display in Video Mode display for normal display.	Short
<p>Note: When use shutdown command, interface shall remain powered in order to receive the turn-on, or wake-up, command.</p>		

DCS command setting		
Data type, hex	Function description	Number of bytes
05/15h	DCS Short Write command is used to write a single data byte to a peripheral such as a display module. If a parameter is not required, the parameter byte shall be 00h.	Short
06h	DCS Read command, the returned data may be of Short or Long packet format.	Short

39h	DCS Long Write/ Write _ LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Long
-----	--	------

Return packet size setting		
Data type, hex	Function description	Number of bytes
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	Short
<p>Note: The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.</p>		

Variable data packet		
Data type, hex	Function description	Number of bytes
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Short
19h	Blanking packet is used to convey blanking timing information in a Long packet.	Short
<p>Note: (1) When Null Packet, the Payload Data belong “null” Data, actual data values sent are irrelevant because the peripheral does not capture or store the data. (2) When Blanking packet, the packet represents a period between active scan lines of a Video Mode display,</p>		

Data stream format – 16bit Format

Data stream format – 16bit Format		
Data type, hex	Function description	Number of bytes
0Eh	Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is five bits red, six bits green, five bits blue, in that order.	Long

The diagram illustrates the bit-level structure of the 16-bit pixel stream. The main packet structure is as follows:

- Packet Header:**
 - Data ID: 1 byte
 - Data Type: 1 byte
 - Virtual Channel: 1 byte
 - Word Count: 2 bytes
 - ECC: 1 byte
- Variable Size Payload:**
 - Pixel 1: 16 bits (5b Red, 6b Green, 5b Blue)
 - ...
 - Pixel n: 16 bits (5b Red, 6b Green, 5b Blue)
- Checksum:** 2 bytes

A detailed view of **Pixel 1** shows the bit layout across two bytes:

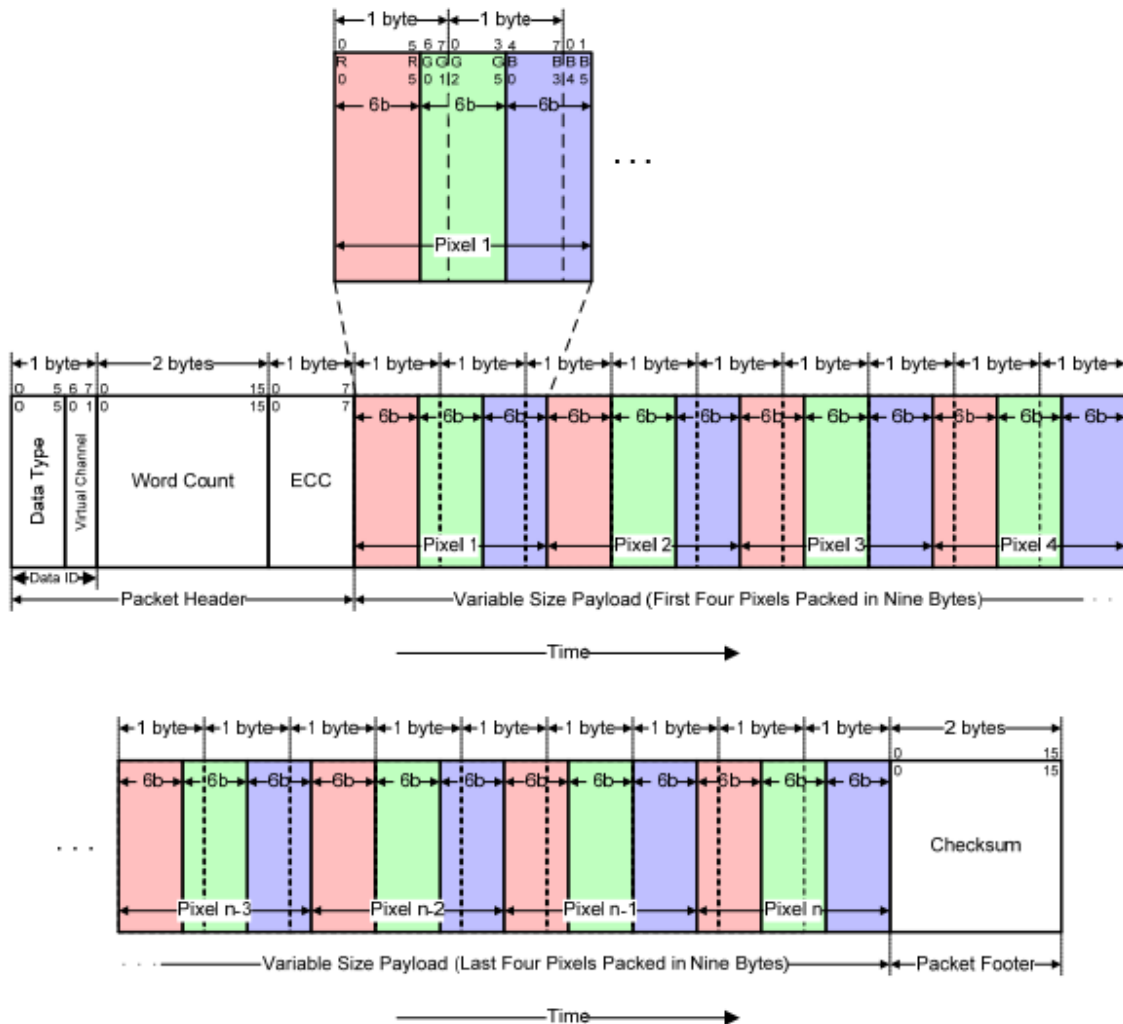
- Byte 1 (bits 0-7):** R (bits 4-0), G (bits 7-2)
- Byte 2 (bits 8-15):** G (bits 1-6), B (bits 7-3)

Time progresses from left to right.

Note: That the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

Data stream format – 18bit Format (mode1)

Data stream format – 18bit Format(Mode1)		
Data type, hex	Function description	Number of bytes
1Eh	Packed Pixel Stream 18-Bit Format is a Long packet used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is six bits red, six bits green, six bits blue, in that order.	Long



Note: Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a “clean start” for the next line.

Data stream format – 18bit Format(mode2)

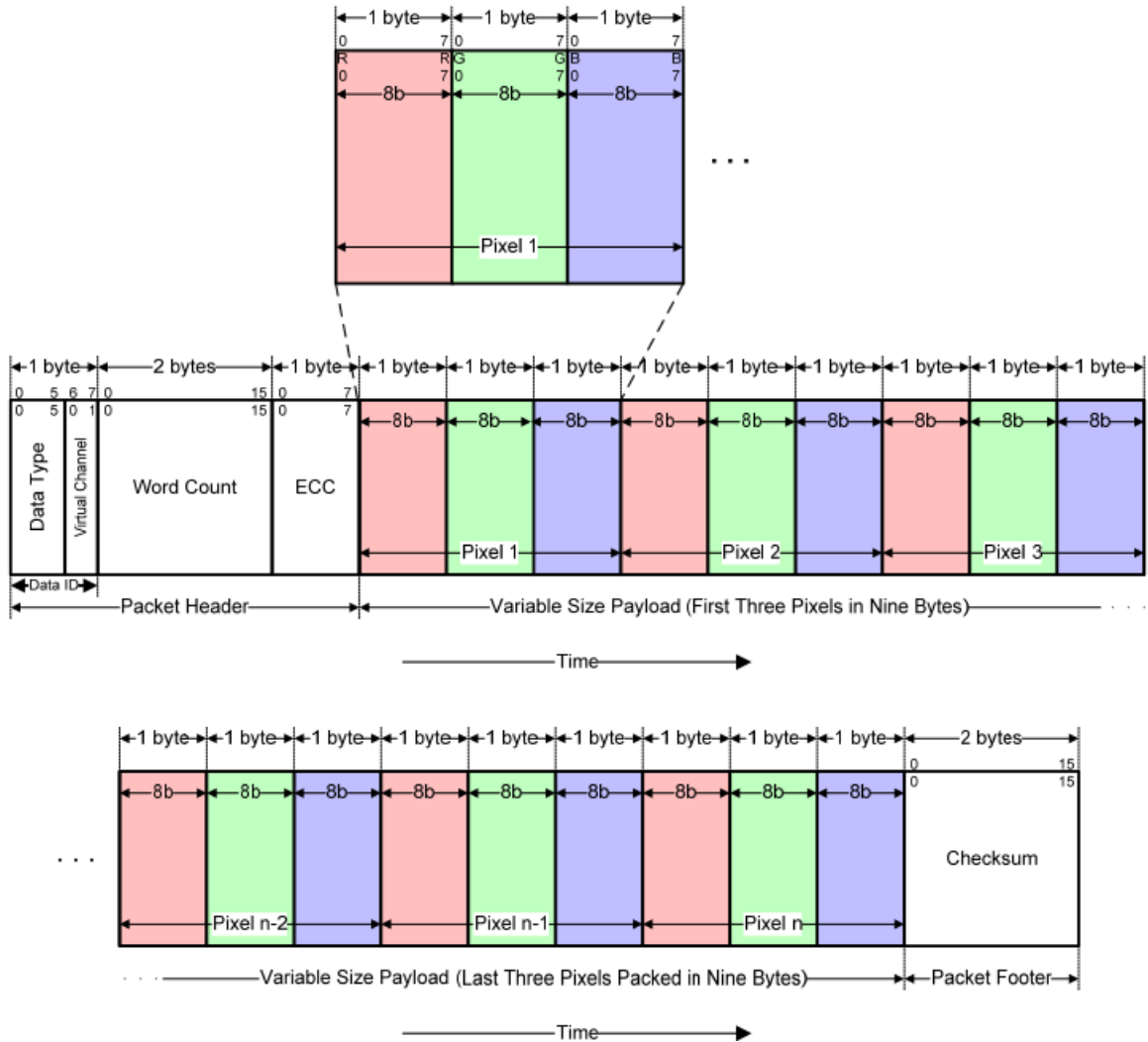
Data stream format – 18bit Format(Mode2)		
Data type, hex	Function description	Number of bytes
2Eh	In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits[1:0] of each payload byte representing active pixels are ignored.	Long

The diagram illustrates the data stream format for 18-bit Pixel Loosely Packed format. It shows a packet structure over time, with a Packet Header and a Variable Size Payload. The Packet Header includes Data ID (1 byte), Data Type (1 byte), Virtual Channel (1 byte), Word Count (2 bytes), and ECC (1 byte). The Variable Size Payload consists of a sequence of 6-bit color components (R, G, B) packed into 1-byte units. Each color component is shifted to the upper bits of the byte, occupying bits [7:2]. The diagram shows the first three pixels (Pixel 1, Pixel 2, Pixel 3) and the last three pixels (Pixel n-2, Pixel n-1, Pixel n) packed in nine bytes. The Packet Footer includes a 2-byte Checksum. The diagram also shows the bit-level details of a single byte, with bits 0-7 and bit positions 0-5 for each color component (R, G, B).

Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

Data stream format – 24bit Format

Data stream format –24bit Format		
Data type, hex	Function description	Number of bytes
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue.	Long



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

1.1.1.14 Peripheral-to-Processor (Reverse Direction) LP Transmissions

All Command Mode systems require bidirectional capability for returning READ data, acknowledge, or error information to the host processor. Multi-Lane systems shall use Lane 0 for all peripheral-to-processor transmissions; other Lanes shall be unidirectional. Reverse-direction signaling shall only use LP (Low Power) mode of transmission.

Peripheral-to-processor transactions are of four basic types:

- ◆ Tearing Effect is a Trigger message sent to convey display timing information to the host processor. Trigger messages are signal byte packets sent by a peripheral's PHY layer in response to a signal from the DSI protocol layer.
- ◆ Acknowledge is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.
- ◆ Acknowledge and Error Report is a Short packet sent if any errors were detected in preceding transmission from the host processor. Once reported, accumulated errors in the error register are cleared.
- ◆ Response to Read Request may be Short or Long packet that returns data requested by the preceding READ command from the processor.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or error information back to the host processor.

Interpretation of processor-to-peripheral transactions with BTA asserted, and the expected responses, are as follows:

- ◆ Following a non-Read command in which no error was detected, the peripheral shall respond with Acknowledge.
- ◆ Following a Read request in which no error was detected, the peripheral shall send the requested READ data.
- ◆ Following a Read request in which the ECC error was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (Acknowledge with Error Report) packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
- ◆ Following a non-Read command in which the ECC error was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (Acknowledge with Error Report) packet, the Error Report shall have the ECC Error flag set.
- ◆ Following any command in which SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid was detected, or the DSI command was not

recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

An error report is a Short packet comprised of two bytes following the DI byte, with an ECC byte following the Error Report bytes. By convention, detection and reporting of each error type is signified by setting the corresponding bit to "1". Table 18 shows the bit assignment for all error reporting.

Bit	Error Report Bit Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

The table as below presents the complete set of peripheral-to-processor Data Types

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge and Error Report	Short
08h	00 1000	End of Transmission packet (EoTp)	Short
11h	01 0001	Generic Short READ Response, 1 byte returned	Short
12h	01 0010	Generic Short READ Response, 2 bytes returned	Short
1Ah	01 1010	Generic Long READ Response	Short
1Ch	01 1100	DCS Long READ Response	Short
21h	10 0001	DCS Short READ Response, 1 byte returned	Short
22h	10 0010	DCS Short READ Response, 2 bytes returned	Short

Data Types for Peripheral-sourced Packets

Acknowledge types		
Data type, hex	Function description	Number of bytes
02h	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes
<p>Note: When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor. With error Acknowledge with error report, Without error Acknowledge.</p>		

Generic Read types		
Data type, hex	Function description	Number of bytes
11h, 12h	This is the Generic Short Read Response, 1 or 2bytes, respectively.	4 bytes
1Ah	This is the long-packet response to Generic Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD + Payload DATA + PF)
<p>Note: If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h.If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent.</p>		

DCS Read types		
Data type, hex	Function description	Number of bytes
21h, 22h	This is the DCS Short Read Response, 1 or 2bytes, respectively..	4 bytes
1Ch	This is the long-packet response to DCS Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD + Payload DATA + PF)
<p>Note: If the peripheral is Checksum capable, it shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h. If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet is sent.</p>		

9 FUNCTION DESCRIPTION

9.1 Display Data RAM

9.1.1 Configuration

The display module has an integrated 360x390x18-bit graphic type static RAM. This 2527200-bit memory allows storing on-chip a 360xRGBx390 image with an 18-bpp resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

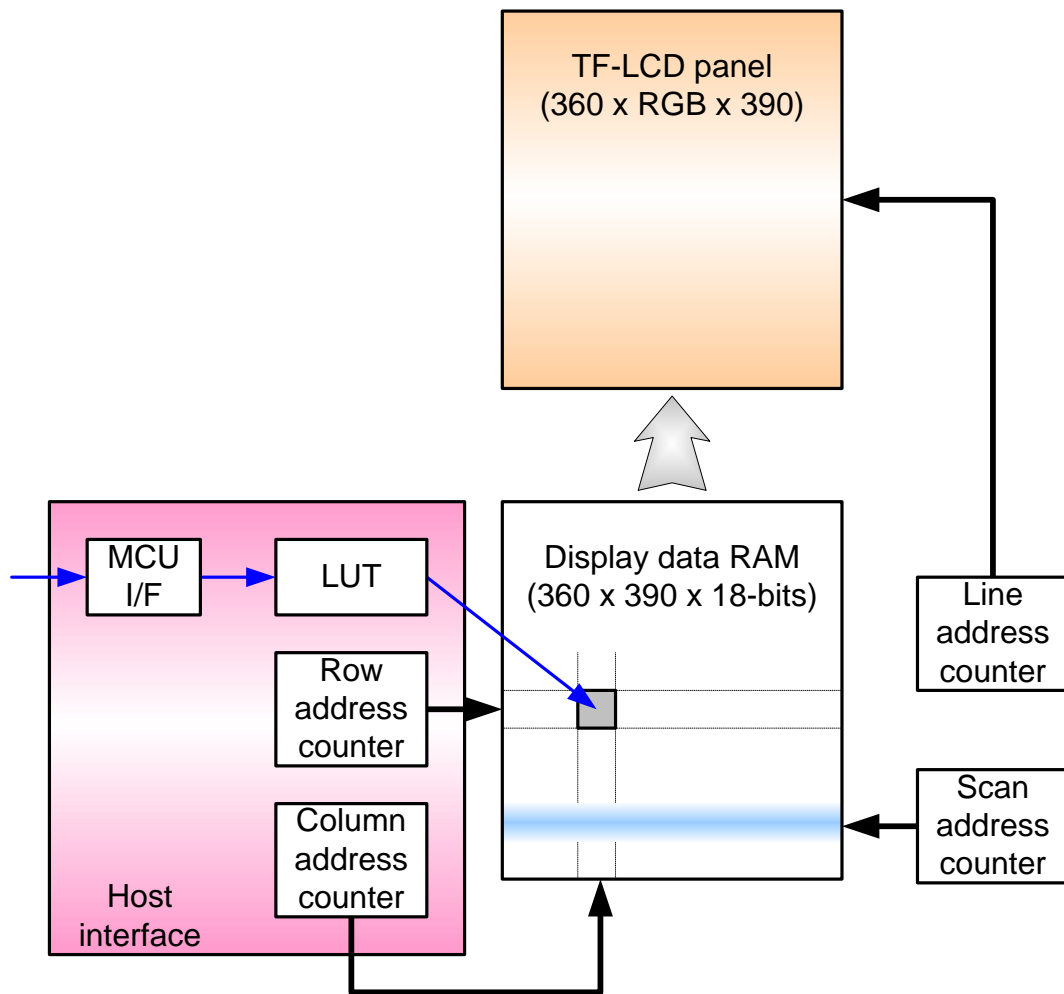


Figure 27 Display data RAM organization

9.1.2 Memory to display address mapping

				RGB alignment									
Data control command				Column									
(MADCTR) MX=0				0			1			359			
				→									
(MADCTR) MX=1				359			358			0			
				←									
Color				R	G	B	R	G	B		R	G	B
Data				R	G	B	R	G	B		R	G	B
Page				R	G	B	R	G	B		R	G	B
(MADCTR) MY=0	(MADCTR) MY=1			R	G	B	R	G	B		R	G	B
0	389												
1	388												
2	387												
3	386												
4	385												
5	384												
6	383												
7	382												
:	:												
382	7			R	G	B	R	G	B		R	G	B
383	6			R	G	B	R	G	B		R	G	B
384	5			R	G	B	R	G	B		R	G	B
385	4			R	G	B	R	G	B		R	G	B
386	3			R	G	B	R	G	B		R	G	B
387	2			R	G	B	R	G	B		R	G	B
388	1			R	G	B	R	G	B		R	G	B
389	0			R	G	B	R	G	B		R	G	B
Source output				0	1	2	3	4	5		1077	1078	1079

9.2 Address Control

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=359 (167h) and Y=0 to Y=389 (185h). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=359 (167h), YE=389 (185h).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET and MADCTL”, define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 8.12 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as below

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

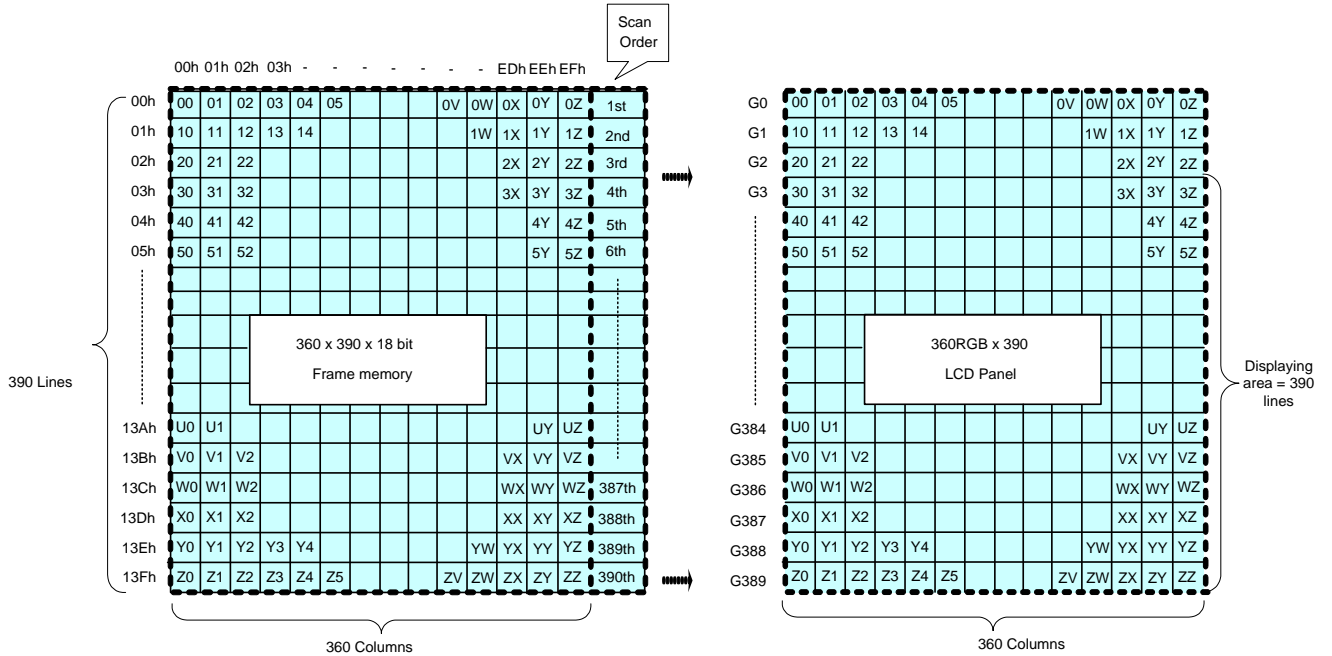
Figure 28 Display data RAM organization

9.3 Normal Display On or Partial Mode On, Vertical Scroll Off

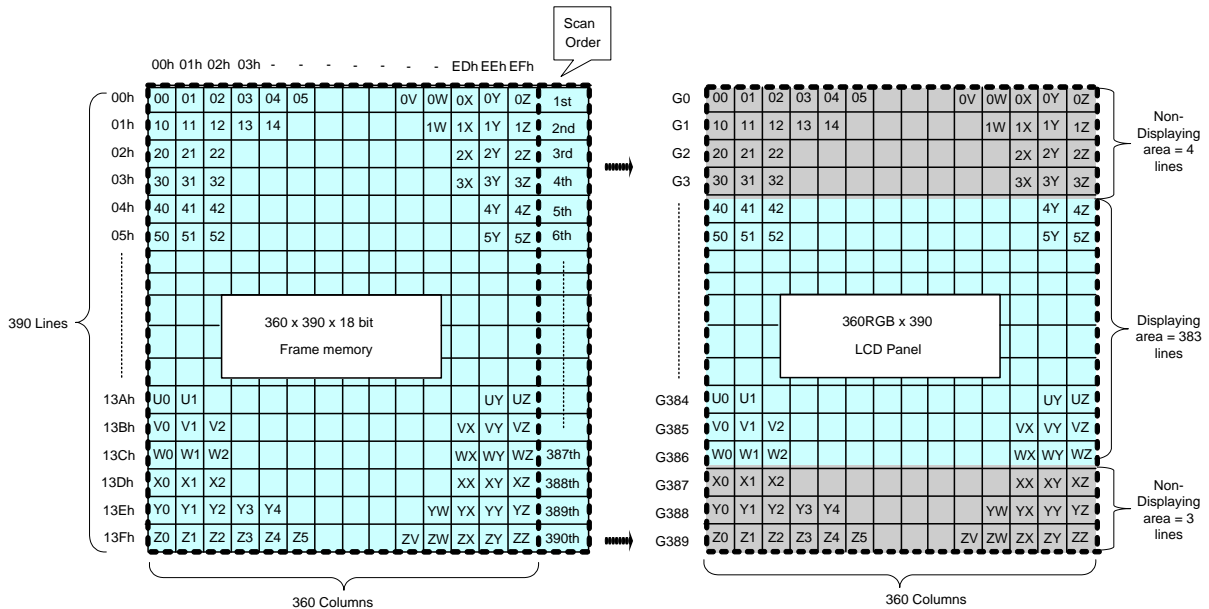
In this mode, contents of the frame memory within an area where column address is 00h to 83h and row address is 00h to 83h is displayed.

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).

Example1) Normal Display On



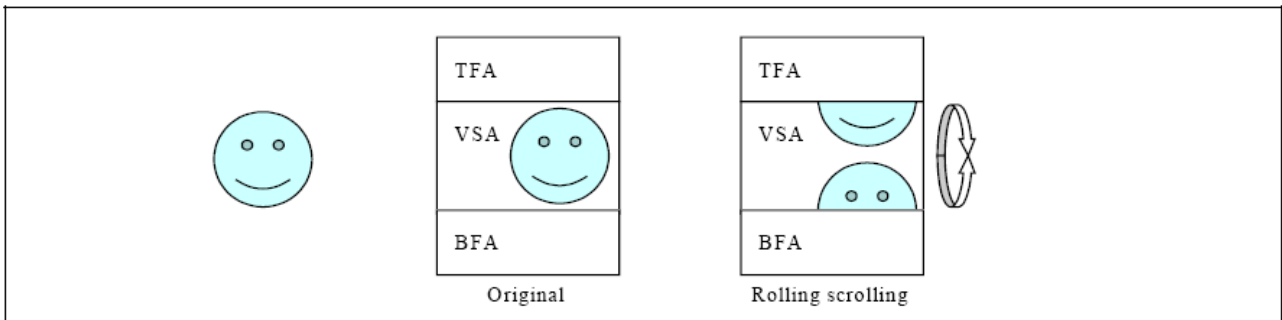
Example2) Partial Display On: PSL[15:0] = 0004h, PEL[15:0] = 013Ch, MADCTR (ML)=0



9.4 Vertical Scroll Mode

9.4.1 Rolling scroll

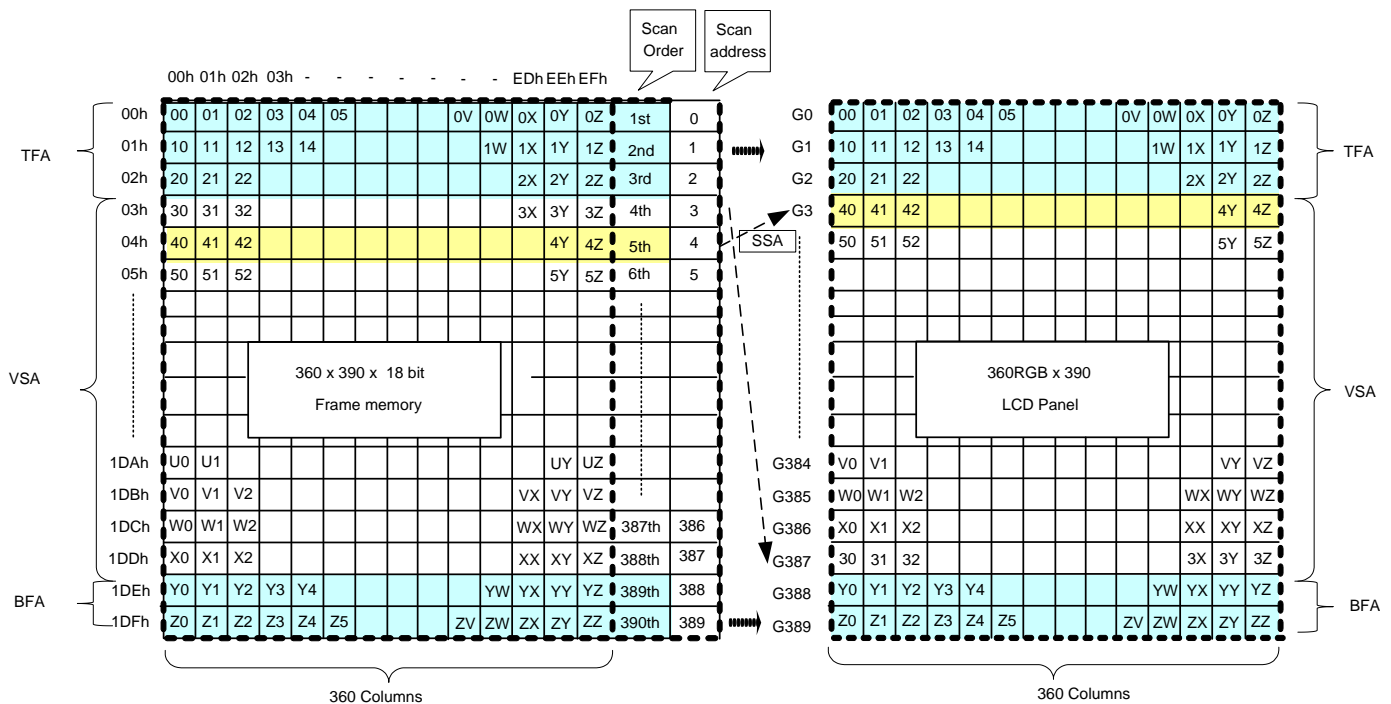
There is just one types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).



Rolling Scroll Definition

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =390. In this case, ‘rolling’ scrolling is applied as shown below. All the memory contents will be used.

Example: Panel size=360 x 390, TFA =3, VSA=385, BFA=2, SSA=4, MADCTR ML=0: Rolling Scroll



9.4.2 Vertical Scroll Example

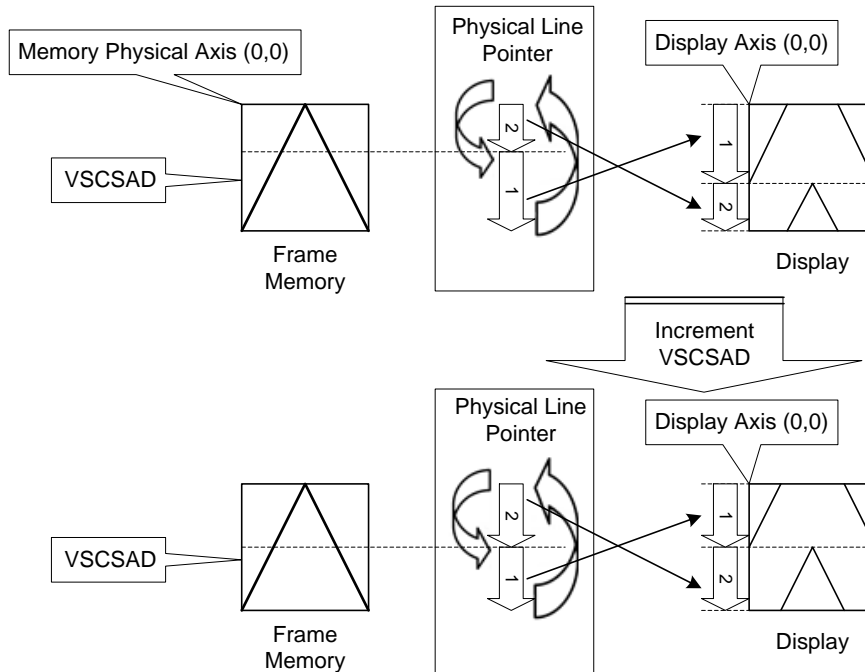
There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

Case 1: $TFA + VSA + BFA \neq$ Panel total scan lines. In this case, scrolling is applied as shown below.

N/A. Do not set $TFA + VSA + BFA \neq$ Panel total scan lines. In that case, unexpected picture will be shown.

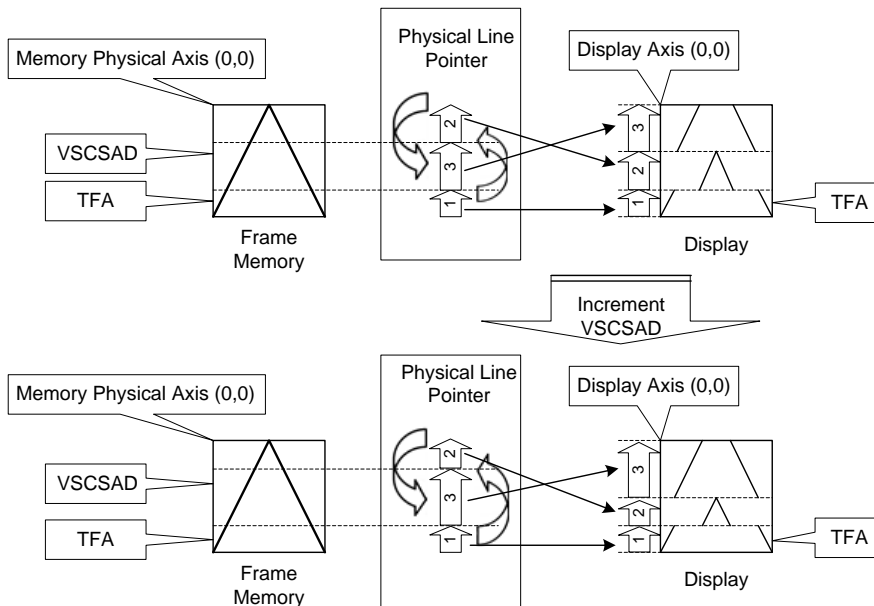
Case 2: $TFA + VSA + BFA =$ Panel total scan lines

Example1) When MADCTR parameter ML="0", TFA=0, VSA=390, BFA=0 and VSCSAD=40.



Display of Vertical Scroll Example 1

Example2) When MADCTR parameter ML="1", TFA=60, VSA=330, BFA=0 and VSCSAD=160.



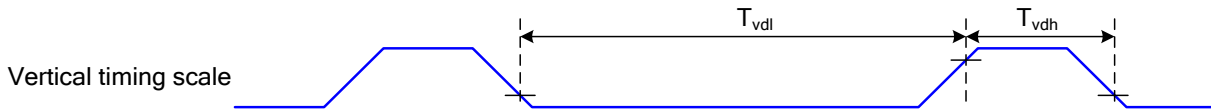
Display of Vertical Scroll Example 2

9.5 Tearing Effect

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

9.5.1 Tearing effect line modes

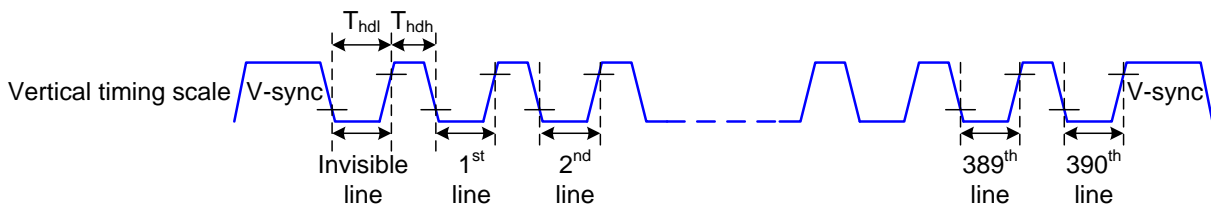
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



tvdh= The LCD display is not updated from the Frame Memory

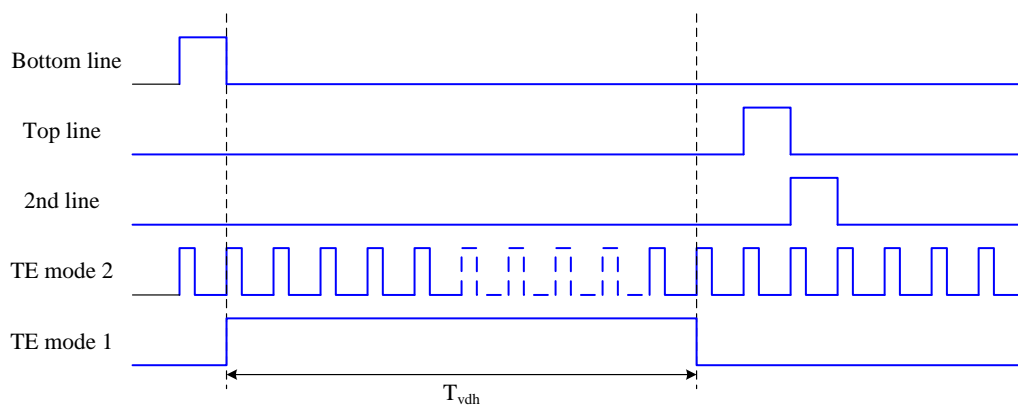
tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 390 H-sync pulses per field.



thdh= The LCD display is not updated from the Frame Memory

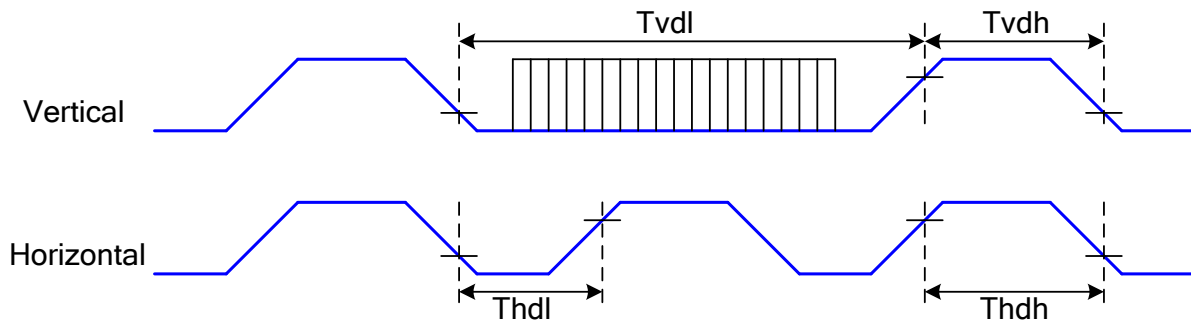
thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

9.5.2 Tearing effect line timings

The Tearing Effect signal is described below:

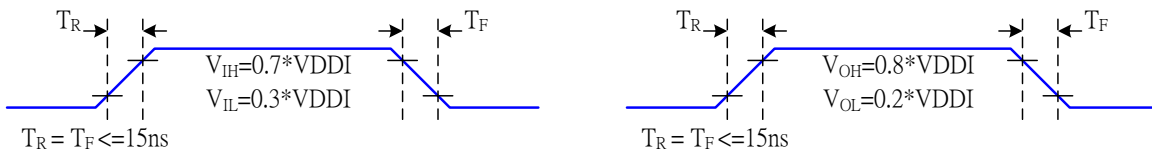


Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	μ s	
thdl	Horizontal Timing Low Duration	16	-	μ s	
thdh	Horizontal Timing High Duration	-	500	μ s	

Table AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25°C)

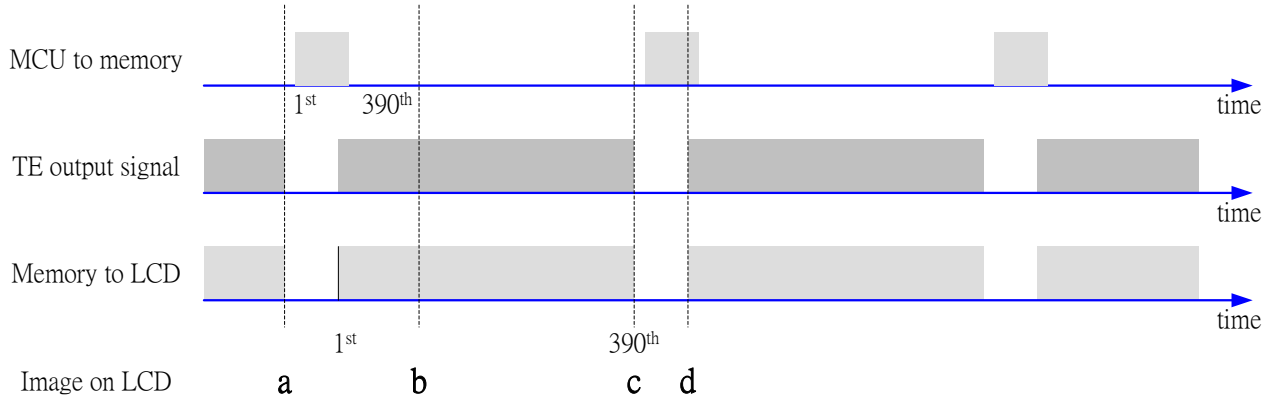
Note: The timings in Table 15 apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.

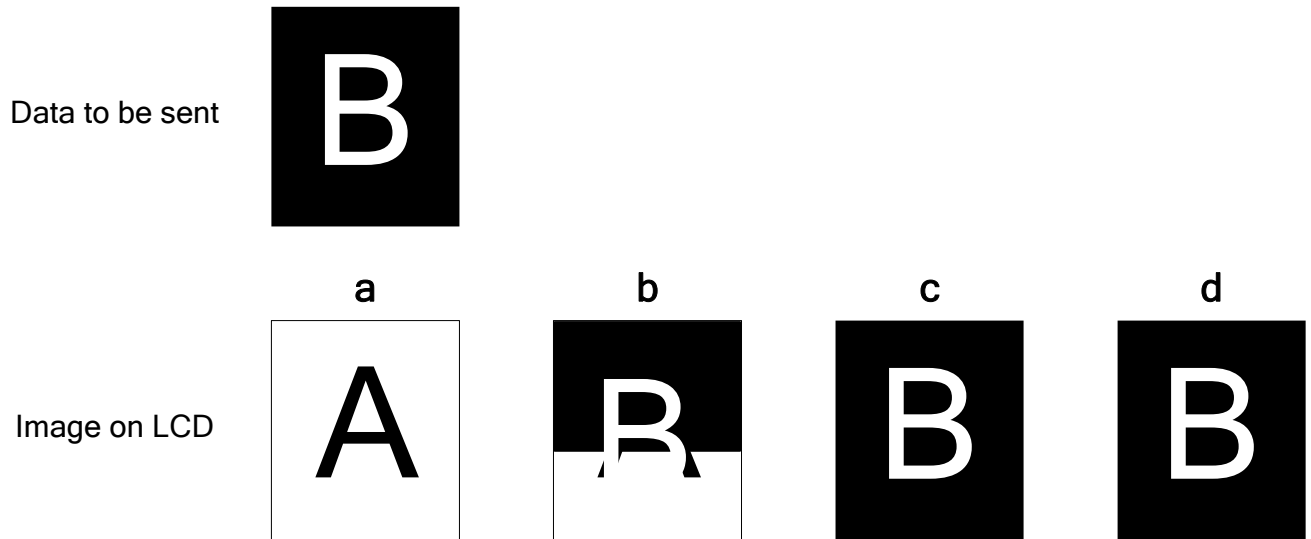


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

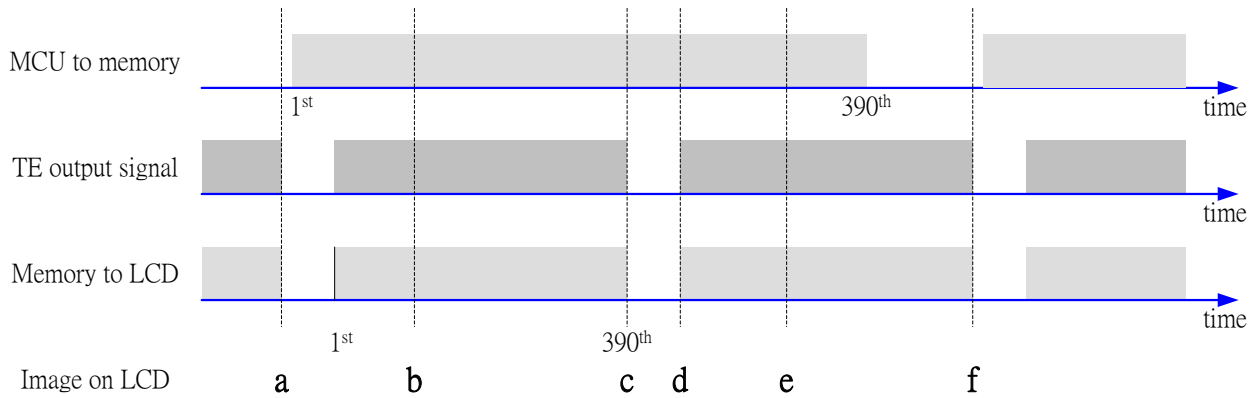
9.5.3 Example 1: MPU Write is faster than panel read



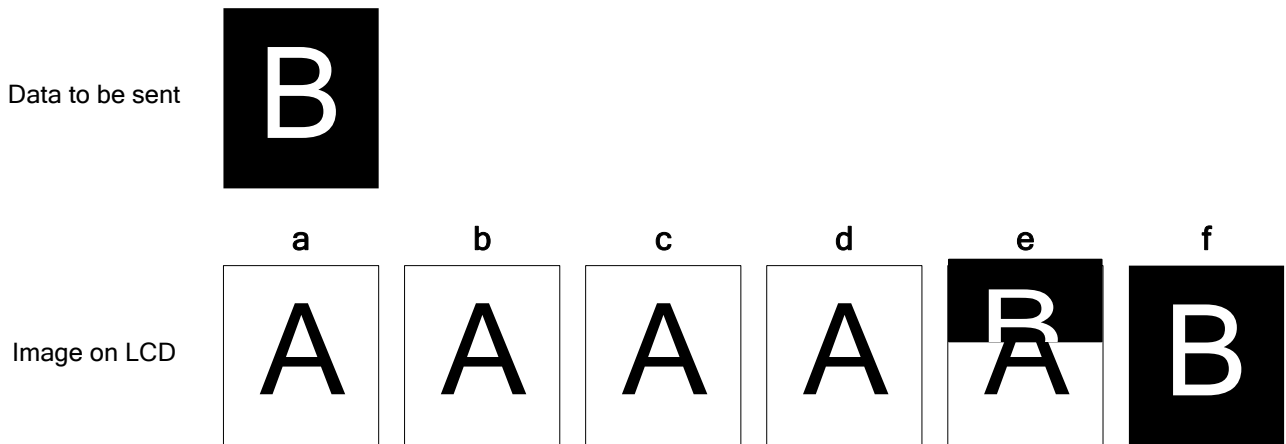
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



9.5.4 Example 2: MPU write is slower than panel read

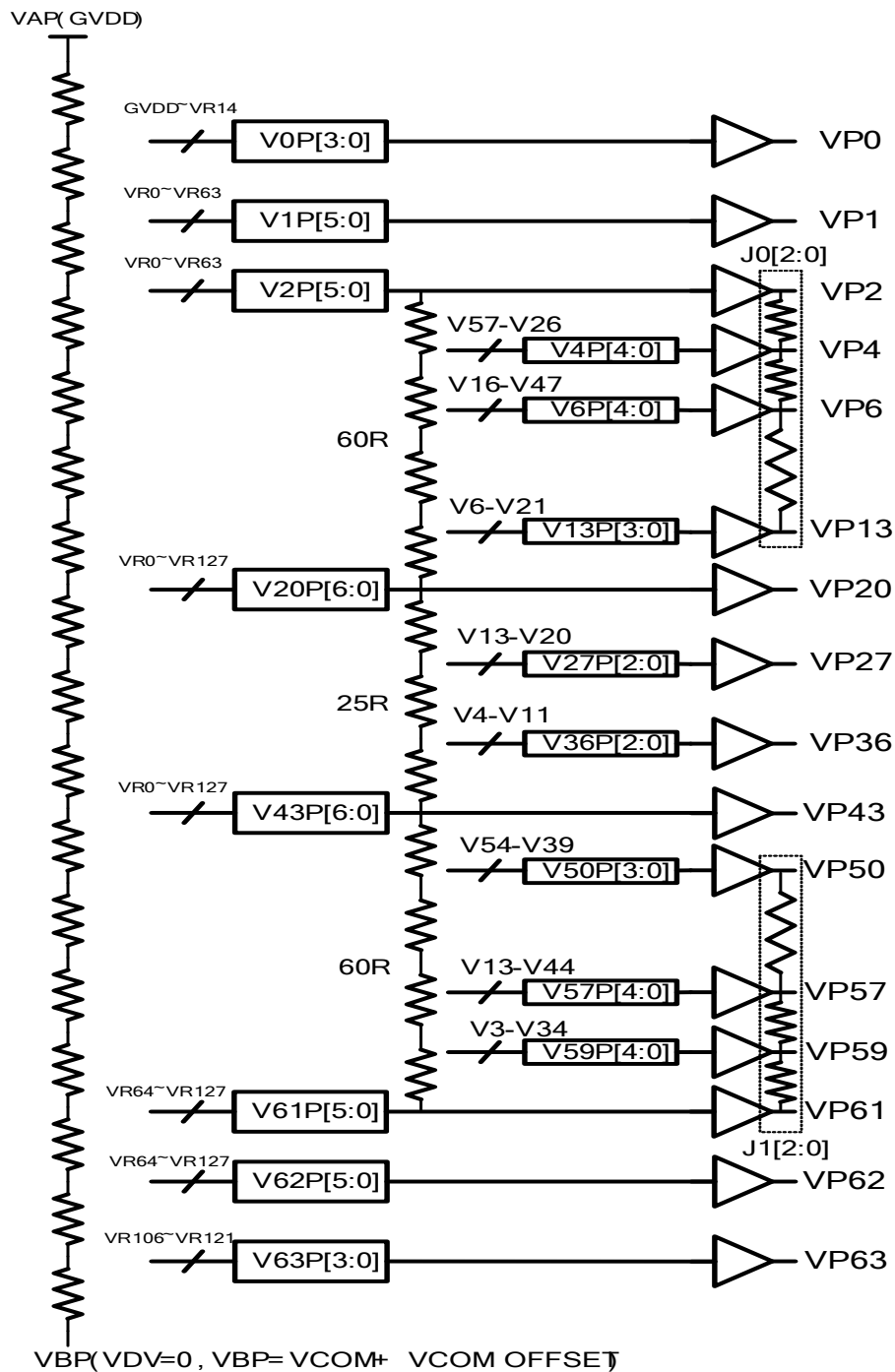


The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.

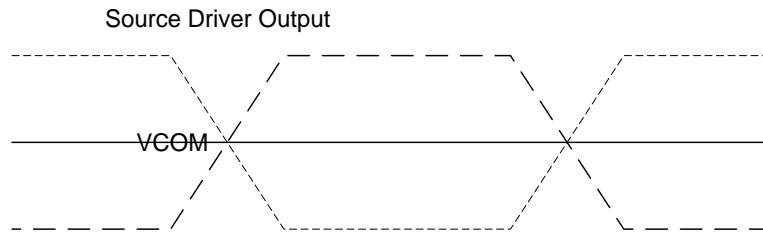


9.6 Gamma Correction

ST77916 incorporate the gamma correction function to display 262K colors for the LCD panel. The gamma correction is performed with 3 groups of registers, which are gradient adjustment, contrast adjustment and fine- adjustment registers for positive and negative polarities.



Gray scale Voltage Generation (Positive)



Relationship between Source Output and VCOM

Percentage adjustment:

VJ0P[2:0], VJ1P[2:0], VJ0N[2:0], VJ1N[2:0] these register are used to adjust the voltage level of interpolation point. The following table is the detail description.

VJ0P[2:0]/VJ0N[2:0]:

	00h	01h	02h	03h	04h	05h	06h	07h
VP3/VN3	50%,18	56%,20	50%,18	60%,22	42%,15	65%,23	45%,16	70%,25
VP5/VN5	50%,18	44%,16	50%,18	42%,15	65%,23	52%,19	40%,14	33%,12
VP7/VN7	86%,30	71%,25	80%,28	66%,23	88%,31	70%,25	76%,27	60%,21
VP8/VN8	71%,25	57%,20	63%,22	49%,17	61%,21	52%,18	58%,20	46%,16
VP9/VN9	57%,20	40%,14	49%,17	34%,12	60%,21	41%,15	47%,16	30%,11
VP10/VN10	43%,15	29%,10	34%,12	23%,8	46%,16	25%,9	36%,13	20%,7
VP11/VN11	29%,10	17%,6	20%,7	14%,5	32%,11	26%,9	23%,8	12%,4
VP12/VN12	14%,5	6%,2	9%,3	6%,2	20%,7	11%,4	17%,6	3%,1

VJ1P[2:0]/VJ1N[2:0]:

	00h	01h	02h	03h	04h	05h	06h	07h
VP51/VN51	86%,30	86%,30	86%,30	89%,31	77%,27	92%,32	83%,29	95%,33
VP52/VN52	71%,25	71%,25	77%,27	80%,28	63%,22	69%,24	75%,26	83%,29
VP53/VN53	57%,20	60%,21	63%,22	69%,24	48%,17	54%,19	66%,23	72%,25
VP54/VN54	43%,15	46%,16	46%,16	51%,18	35%,12	41%,14	55%,19	60%,21
VP55/VN55	29%,10	34%,12	31%,11	37%,13	23%,8	40%,14	26%,9	43%,15
VP56/VN56	14%,5	17%,6	14%,5	20%,7	9%,3	23%,8	11%,4	26%,9
VP58/VN58	50%,18	56%,20	47%,17	47%,17	53%,19	59%,21	45%,16	42%,15
VP60/VN60	50%,18	50%,18	50%,18	53%,19	42%,15	45%,16	55%,20	60%,21

voltage level percentage adjustment description

Source voltage of positive gamma level

Gamma level	Related Register	Formula
VP0	V0P[3:0]	$(VAP-VBP)*(129R-V0P[3:0]R)/129R+VBP$
VP1	V1P[5:0]	$(VAP-VBP)*(128R-V1P[5:0]R)/129R+VBP$
VP2	V2P[5:0]	$(VAP-VBP)*(128R-V2P[5:0]R)/129R+VBP$
VP3	VJ0P[2:0]	$(VP2-VP4)*VJ0P[2:0]+VP4$
VP4	V4P[4:0]	$(VP2-VP20)*(57R-V4P[4:0])/60R+VP20$
VP5	VJ0P[2:0]	$(VP4-VP6)*VJ0P[2:0]+VP6$
VP6	V6P[4:0]	$(VP2-VP20)*(47R-V6P[4:0])/60R+VP20$
VP7	VJ0P[2:0]	$(VP6-VP13)*VJ0P[2:0]+VP13$
VP8	VJ0P[2:0]	$(VP6-VP13)*VJ0P[2:0]+VP13$
VP9	VJ0P[2:0]	$(VP6-VP13)*VJ0P[2:0]+VP13$
VP10	VJ0P[2:0]	$(VP6-VP13)*VJ0P[2:0]+VP13$
VP11	VJ0P[2:0]	$(VP6-VP13)*VJ0P[2:0]+VP13$
VP12	VJ0P[2:0]	$(VP6-VP13)*VJ0P[2:0]+VP13$
VP13	V13P[3:0]	$(VP2-VP20)*(21R-V13P[3:0])/60R+VP20$
VP14	--	$(VP13-VP20)/(20-13)*(20-14)+VP20$
VP15	--	$(VP13-VP20)/(20-13)*(20-15)+VP20$
VP16	--	$(VP13-VP20)/(20-13)*(20-16)+VP20$
VP17	--	$(VP13-VP20)/(20-13)*(20-17)+VP20$
VP18	--	$(VP13-VP20)/(20-13)*(20-18)+VP20$
VP19	--	$(VP13-VP20)/(20-13)*(20-19)+VP20$
VP20	V20P[6:0]	$(VAP-VBP)*(128R-V20P[6:0]R)/129R+VBP$
VP21	--	$(VP20-VP27)/(27-20)*(27-21)+VP27$
VP22	--	$(VP20-VP27)/(27-20)*(27-22)+VP27$
VP23	--	$(VP20-VP27)/(27-20)*(27-23)+VP27$
VP24	--	$(VP20-VP27)/(27-20)*(27-24)+VP27$
VP25	--	$(VP20-VP27)/(27-20)*(27-25)+VP27$
VP26	--	$(VP20-VP27)/(27-20)*(27-26)+VP27$
VP27	V27P[2:0]	$(VP20-VP43)*(20R-V27P[2:0])/25R+VP43$
VP28	--	$(VP27-VP36)/(36-27)*(36-28)+VP36$
VP29	--	$(VP27-VP36)/(36-27)*(36-29)+VP36$
VP30	--	$(VP27-VP36)/(36-27)*(36-30)+VP36$
VP31	--	$(VP27-VP36)/(36-27)*(36-31)+VP36$
VP32	--	$(VP27-VP36)/(36-27)*(36-32)+VP36$
VP33	--	$(VP27-VP36)/(36-27)*(36-33)+VP36$
VP34	--	$(VP27-VP36)/(36-27)*(36-34)+VP36$
VP35	--	$(VP27-VP36)/(36-27)*(36-35)+VP36$
VP36	V36P[2:0]	$(VP20-VP43)*(11R-V36P[2:0])/25R+VP43$
VP37	--	$(VP36-VP43)/(43-36)*(43-37)+VP43$
VP38	--	$(VP36-VP43)/(43-36)*(43-38)+VP43$
VP39	--	$(VP36-VP43)/(43-36)*(43-39)+VP43$
VP40	--	$(VP36-VP43)/(43-36)*(43-40)+VP43$
VP41	--	$(VP36-VP43)/(43-36)*(43-41)+VP43$
VP42	--	$(VP36-VP43)/(43-36)*(43-42)+VP43$
VP43	V43P[6:0]	$(VAP-VBP)*(128R-V43P[6:0]R)/129R+VBP$
VP44	--	$(VP43-VP50)/(50-43)*(50-44)+VP50$
VP45	--	$(VP43-VP50)/(50-43)*(50-45)+VP50$
VP46	--	$(VP43-VP50)/(50-43)*(50-46)+VP50$
VP47	--	$(VP43-VP50)/(50-43)*(50-47)+VP50$
VP48	--	$(VP43-VP50)/(50-43)*(50-48)+VP50$
VP49	--	$(VP43-VP50)/(50-43)*(50-49)+VP50$
VP50	V50P[3:0]	$(VP43-VP61)*(54R-V50P[3:0])/60R+VP61$
VP51	VJ1P[2:0]	$(V5P0-VP57)*VJ1P[2:0]+VP57$
VP52	VJ1P[2:0]	$(VP50-VP57)*VJ1P[2:0]+VP57$

VP53	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP54	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP55	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP56	VJ1P[2:0]	(VP50-VP57)* VJ1P[2:0]+VP57
VP57	V57P[4:0]	(VP43-VP61)*(44R-V57P[4:0])/60R+VP61
VP58	VJ1P[2:0]	(VP57-VP59)* VJ1P[2:0]+VP59
VP59	V59P[4:0]	(VP43-VP61)*(34R-V59P[4:0])/60R+VP61
VP60	VJ1P[2:0]	(VP59-VP61)* VJ1P[2:0]+VP61
VP61	V61P[5:0]	(VAP-VBP)*(64R-V61P[5:0]R)/129R+VBP
VP62	V62P[5:0]	(VAP-VBP)*(64R-V62P[5:0]R)/129R+VBP
VP63	V63P[3:0]	(VAP-VBP)*(23R-V63P[3:0]R)/129R+VBP

Source voltage of negative gamma level

Gamma level	Related Register	Formula
VN0	V0N[3:0]	VBN-(VBN-VAN)*(129R-V0N[3:0]R)/129R
VN1	V1N[5:0]	VBN-(VBN-VAN)*(128R-V1N[5:0]R)/129R
VN2	V2N[5:0]	VBN-(VBN-VAN)*(128R-V2N[5:0]R)/129R
VN3	VJ0N[2:0]	(VN2-VN4)* VJ0N[2:0]+VN4
VN4	V4N[4:0]	(VN2-VN20)*(57R-V4N[4:0])/60R+VN20
VN5	VJ0N[2:0]	(VN4-VN6)* VJ0N[2:0]+VN6
VN6	V6N[4:0]	(VN2-VN20)*(47R-V6N[4:0])/60R+VN20
VN7	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN8	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN9	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN10	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN11	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN12	VJ0N[2:0]	(VN6-VN13)* VJ0N[2:0]+VN13
VN13	V13N[3:0]	(VN2-VN20)*(21R-V13N[3:0])/60R+VN20
VN14	--	(VN13-VN20)/(20-13)*(20-14)+VN20
VN15	--	(VN13-VN20)/(20-13)*(20-15)+VN20
VN16	--	(VN13-VN20)/(20-13)*(20-16)+VN20
VN17	--	(VN13-VN20)/(20-13)*(20-17)+VN20
VN18	--	(VN13-VN20)/(20-13)*(20-18)+VN20
VN19	--	(VN13-VN20)/(20-13)*(20-19)+VN20
VN20	V20N[6:0]	VBN-(VBN-VAN)*(128R-V20N[6:0]R)/129R
VN21	--	(VN20-VN27)/(27-20)*(27-21)+VN27
VN22	--	(VN20-VN27)/(27-20)*(27-22)+VN27
VN23	--	(VN20-VN27)/(27-20)*(27-23)+VN27
VN24	--	(VN20-VN27)/(27-20)*(27-24)+VN27
VN25	--	(VN20-VN27)/(27-20)*(27-25)+VN27
VN26	--	(VN20-VN27)/(27-20)*(27-26)+VN27
VN27	V27N[2:0]	(VN20-VN43)*(20R-V27N[2:0])/25R+VN43
VN28	--	(VN27-VN36)/(36-27)*(36-28)+VN36
VN29	--	(VN27-VN36)/(36-27)*(36-29)+VN36
VN30	--	(VN27-VN36)/(36-27)*(36-30)+VN36
VN31	--	(VN27-VN36)/(36-27)*(36-31)+VN36
VN32	--	(VN27-VN36)/(36-27)*(36-32)+VN36
VN33	--	(VN27-VN36)/(36-27)*(36-33)+VN36
VN34	--	(VN27-VN36)/(36-27)*(36-34)+VN36
VN35	--	(VN27-VN36)/(36-27)*(36-35)+VN36
VN36	V36N[2:0]	(VN20-VN43)*(11R-V36N[2:0])/25R+VN43
VN37	--	(VN36-VN43)/(43-36)*(43-37)+VN43
VN38	--	(VN36-VN43)/(43-36)*(43-38)+VN43
VN39	--	(VN36-VN43)/(43-36)*(43-39)+VN43

VN40	--	$(VN36-VN43)/(43-36)*(43-40)+VN43$
VN41	--	$(VN36-VN43)/(43-36)*(43-41)+VN43$
VN42	--	$(VN36-VN43)/(43-36)*(43-42)+VN43$
VN43	V43N[6:0]	$VBN-(VBN-VAN)*(128R-V43N[6:0]R)/129R$
VN44	--	$(VN43-VN50)/(50-43)*(50-44)+VN50$
VN45	--	$(VN43-VN50)/(50-43)*(50-45)+VN50$
VN46	--	$(VN43-VN50)/(50-43)*(50-46)+VN50$
VN47	--	$(VN43-VN50)/(50-43)*(50-47)+VN50$
VN48	--	$(VN43-VN50)/(50-43)*(50-48)+VN50$
VN49	--	$(VN43-VN50)/(50-43)*(50-49)+VN50$
VN50	V50N[3:0]	$(VN43-VN61)*(54R-V50N[3:0])/60R+VN61$
VN51	VJ1N[2:0]	$(V5N0-VN57)*VJ1N[2:0]+VN57$
VN52	VJ1N[2:0]	$(VN50-VN57)*VJ1N[2:0]+VN57$
VN53	VJ1N[2:0]	$(VN50-VN57)*VJ1N[2:0]+VN57$
VN54	VJ1N[2:0]	$(VN50-VN57)*VJ1N[2:0]+VN57$
VN55	VJ1N[2:0]	$(VN50-VN57)*VJ1N[2:0]+VN57$
VN56	VJ1N[2:0]	$(VN50-VN57)*VJ1N[2:0]+VN57$
VN57	V57N[4:0]	$(VN43-VN61)*(44R-V57N[4:0])/60R+VN61$
VN58	VJ1N[2:0]	$(VN57-VN59)*VJ1N[2:0]+VN59$
VN59	V59N[4:0]	$(VN43-VN61)*(34R-V59N[4:0])/60R+VN61$
VN60	VJ1N[2:0]	$(VN59-VN61)*VJ1N[2:0]+VN61$
VN61	V61N[5:0]	$VBN-(VBN-VAN)*(64R-V61N[5:0]R)/129R$
VN62	V62N[5:0]	$VBN-(VBN-VAN)*(64R-V62N[5:0]R)/129R$
VN63	V63N[3:0]	$VBN-(VBN-VAN)*(23R-V63N[3:0]R)/129R$

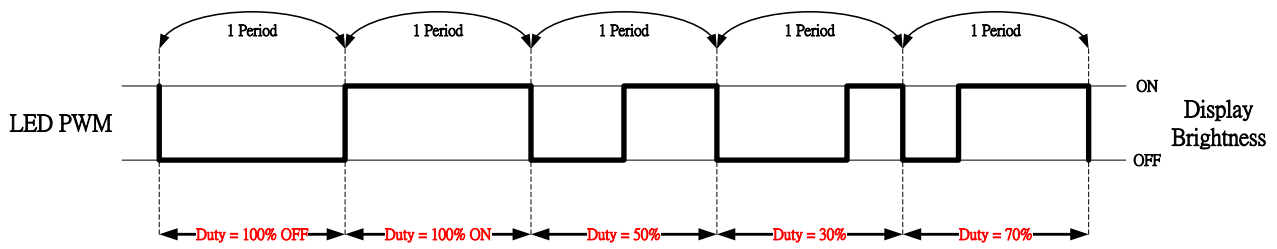
9.7 Brightness Control Block

There is an external output signal from brightness block, LEDPWM to control the LED driver IC in order to control display brightness.

There are register bits, R51h, DBV[7:0] for display brightness of manual brightness setting. The LEDPWM duty is calculated as $DBV[7:0] / 255 \times \text{Period}$ (affected by OSC frequency).

For example: LEDPWM period = 3 ms, and $DBV[7:0] = '200'$. Then LEDPWM duty = $200 / 255 = 78.1\%$.

Correspond to the LEDPWM period = 3 ms, the high-level of LEDPWM (high effective) = 2.344 ms, and the low-level of LEDPWM = 0.656 m



LEDPWM Output Duty

10 POWER DEFINITION

10.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Normal Mode Off (full display), Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Normal Mode Off (full display), Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode

In this mode, the DC:DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

6. Power Off Mode

In this mode, both VDD and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

10.2 Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

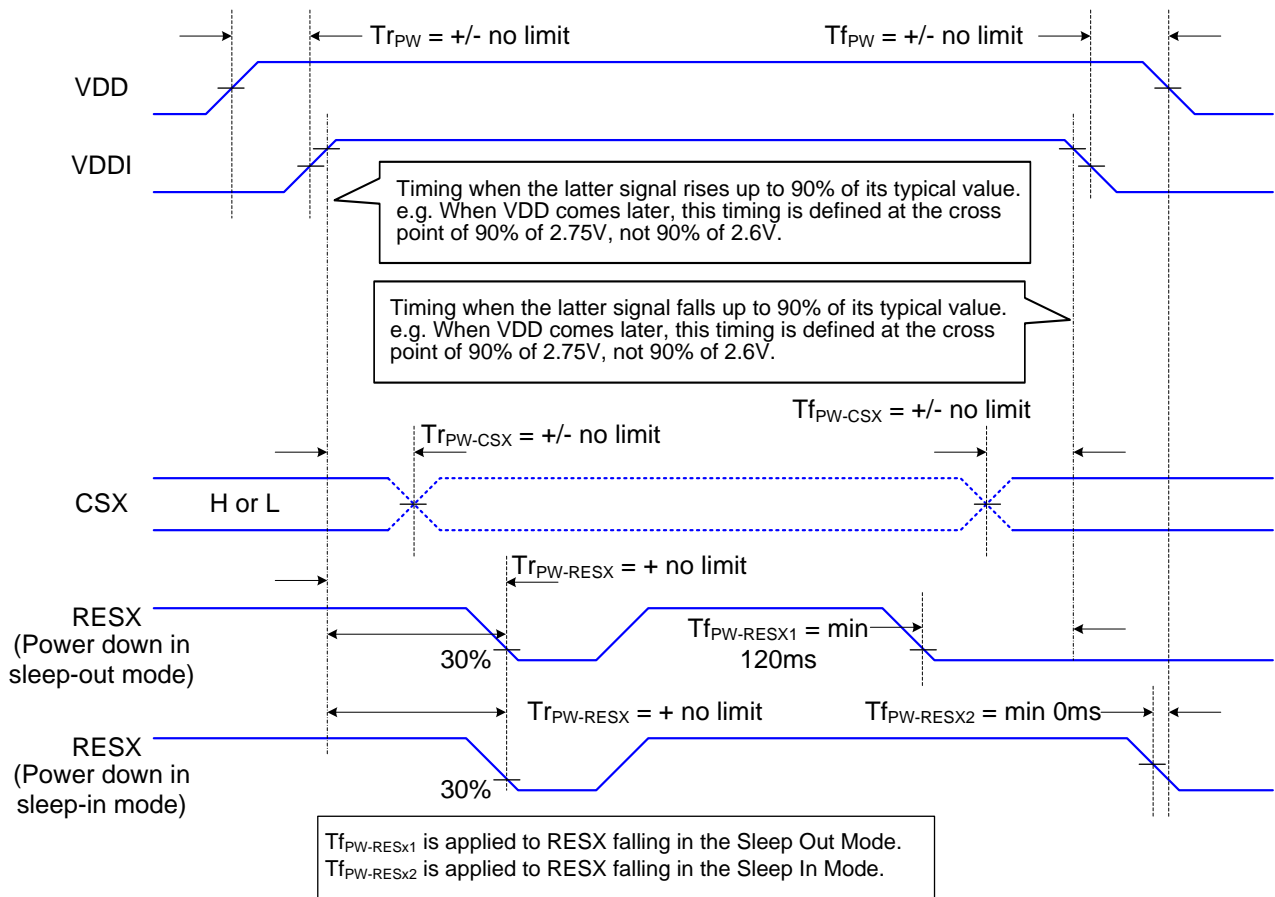
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



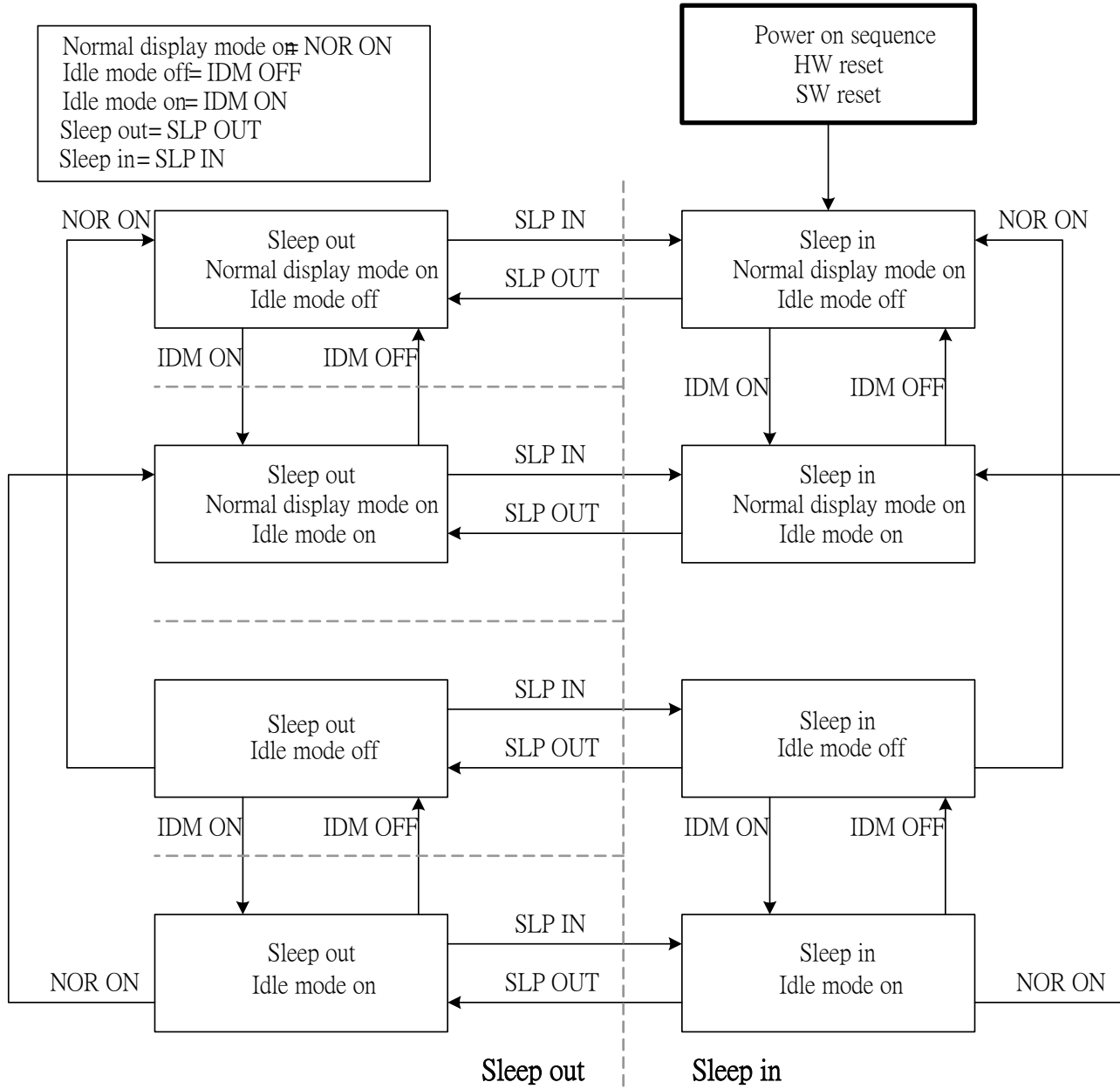
10.3 Uncontrolled Power OFF

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

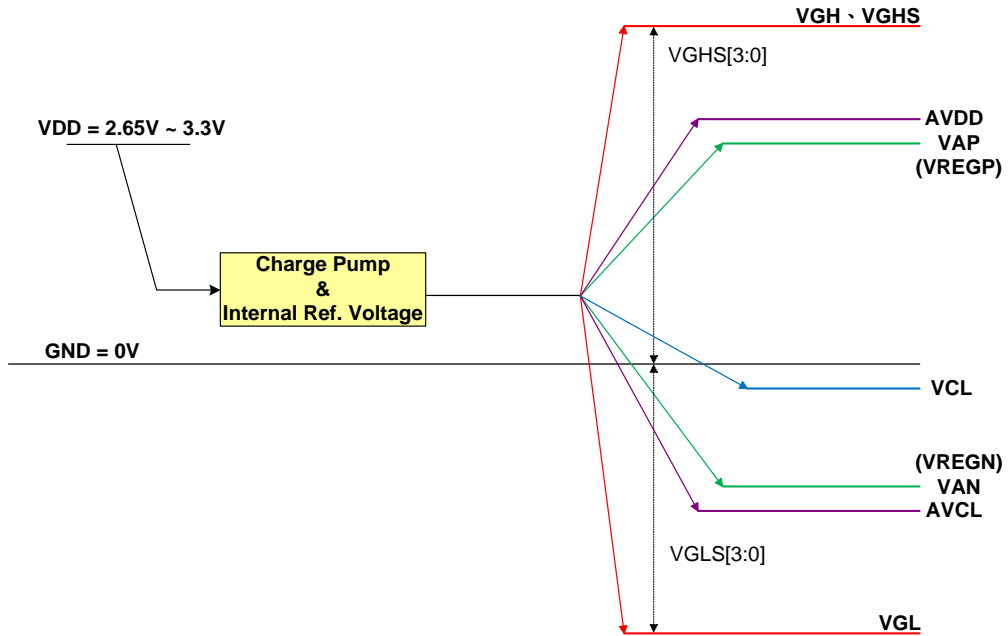
If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display

(blank display) and remains blank until "Power On Sequence" powers it up.

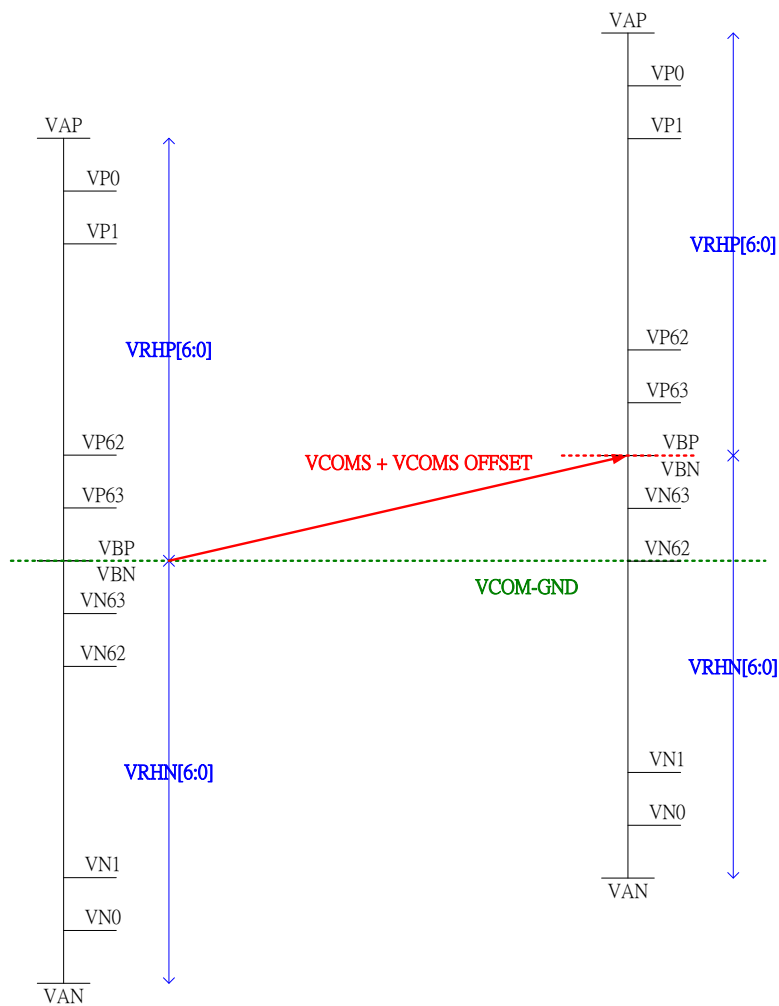
10.4 Power Flow Chart



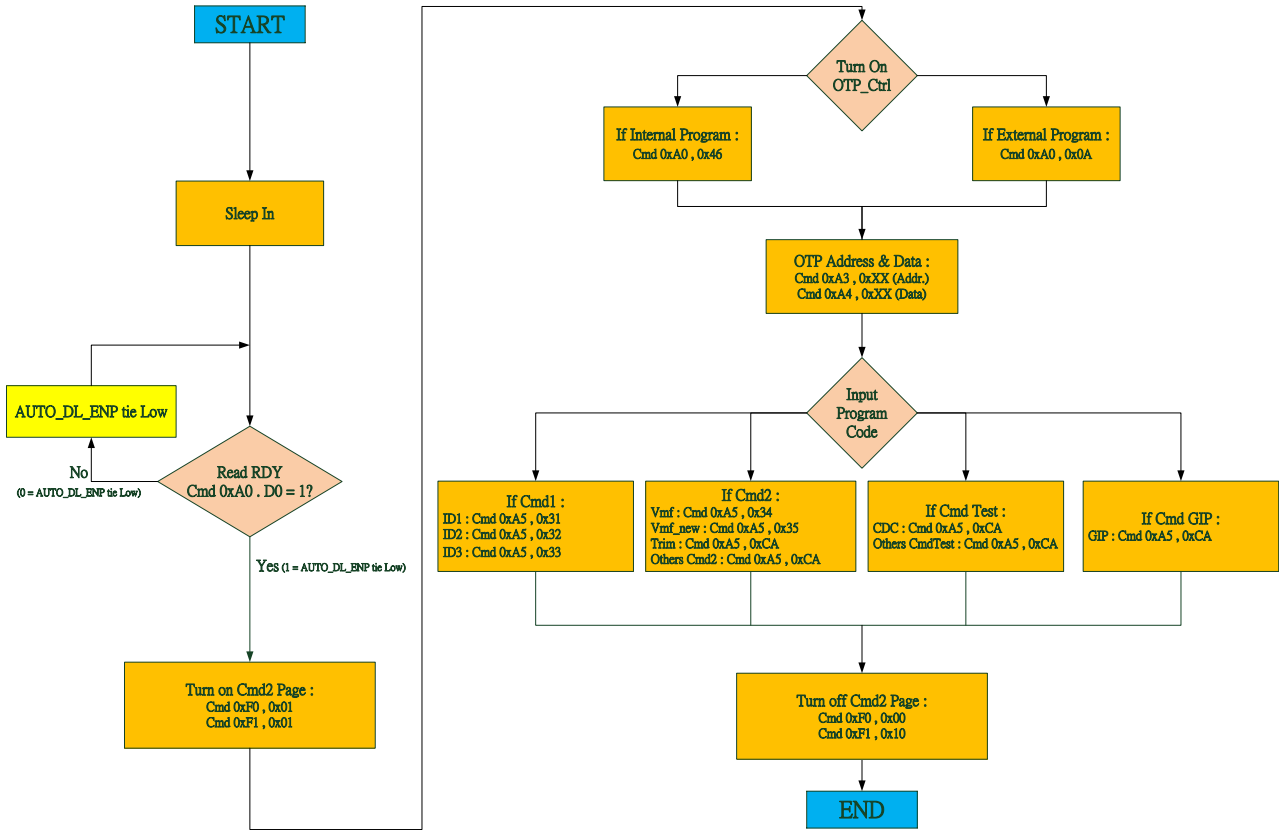
10.5 Voltage Generation



10.6 Relationship about source voltage

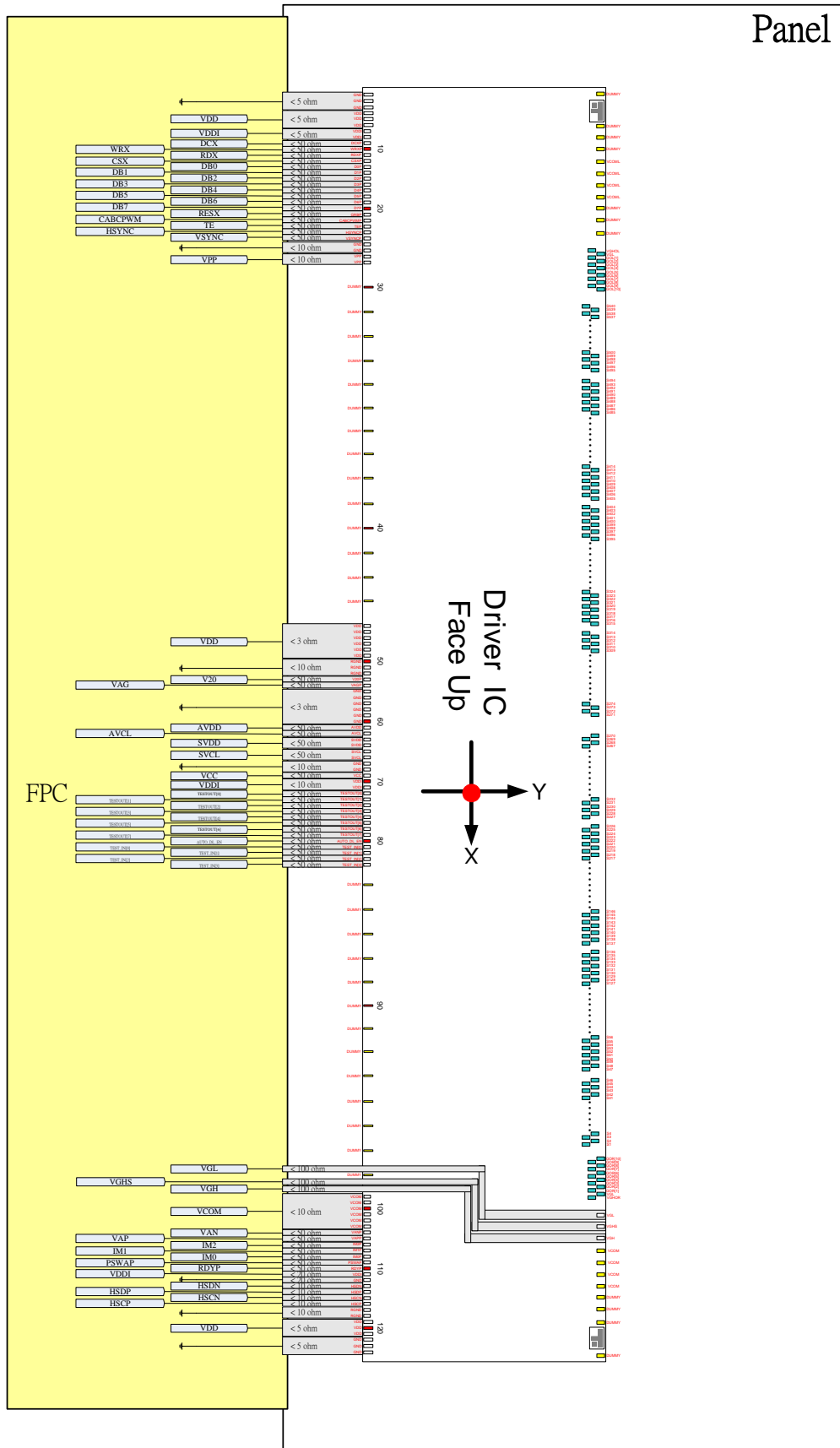


11 NVM PROGRAMMING FLOW



12 APPLICATION NOTE

12.1 Layout Resistance Suggestion



13 COMMAND

13.1 Page Set Table

PAGE SET Table														
Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
CSC	0	↑	1	-	1	1	1	1	0	0	0	0	(F0h)	Command
	1	↑	1		-	CDC_EN	-	GIP_EN	TEST_EN	-	GAM_EN	CMD2_EN		
CSC	0	↑	1	-	1	1	1	1	0	0	0	1	(F1h)	Command
	1	↑	1		-	-	-	CMD2_xP ROT2	-	-	-	CMD2_PR OT1		
CSC	0	↑	1	-	1	1	1	1	0	0	1	0	(F2h)	Command
	1	↑	1		TST_xPR OT1	CDC_PRO T1	-	-	TST_PRO T1	CDC_xPR OT1	-	-		
CSC	0	↑	1	-	1	1	1	1	0	0	1	1	(F3h)	Command
	1	↑	1		-	-	-	GIP_PRO T2	-	-	-	GIP_xPRO T1		
SPIOR	0	↑	1		1	1	1	1	0	1	0	0	(F4h)	SPI Others Read

CSC1 (F0h): Command Set Ctrl 1

F0H	Command Set Ctrl 1												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CK	0	↑	1	-	1	1	1	1	0	0	0	0	(F0h)
parameter	1	↑	1	-	-	CDC_EN	-	GIP_EN	TEST_EN	-	GAM_EN	CMD2_EN	(00h)
Description	F0	F1	F2	F3	Description								
	00	-	-	-	Command2 disable · Gamma Command disable · Test Command disable · CDC Command disable · GIP Command disable								
	02	-	-	-	Gamma enable								
	01	01	-	-	Command2 page enable								
	08	-	08	-	Test Command page enable								
	80	-	40	-	CDC Command page enable								
	10	-	-	10	GIP Command page enable								
': Don't care.													
Register availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Sleep In						Yes							
Default	Status						Default Value						
	Power On Sequence						00h						
	S/W Reset						00h						
	H/W Reset						00h						

CSC2 (F1h): Command Set Ctrl 2

F1H	Command Set Ctrl 2												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CK	0	↑	1	-	1	1	1	1	0	0	0	1	(F1h)
parameter	1	↑	1	-	-	-	-	CMD2_xPROT2	-	-	-	CMD2_PROT1	(10h)

Description	F0	F1	F2	F3	Description
	00	-	-	-	Command2 disable \ Gamma Command disable \ Test Command disable \ CDC Command disable \ GIP Command disable
	02	-	-	-	Gamma enable
	01	01	-	-	Command2 page enable
	08	-	08	-	Test Command page enable
	80	-	40	-	CDC Command page enable
	10	-	-	10	GIP Command page enable
⌚: Don't care.					
Register availability	Status				Availability
	Normal Mode On, Idle Mode Off, Sleep Out				Yes
	Normal Mode On, Idle Mode On, Sleep Out				Yes
	Partial Mode On, Idle Mode Off, Sleep Out				Yes
	Partial Mode On, Idle Mode On, Sleep Out				Yes
Sleep In				Yes	
Default	Status		Default Value		
	Power On Sequence		10h		
	S/W Reset		10h		
	H/W Reset		10h		

CSC3 (F2h): Command Set Ctrl 3

F2H	Command Set Ctrl 3												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CK	0	↑	1	-	1	1	1	1	0	0	1	0	(F2h)
parameter	1	↑	1	-	TST_xPROT2	CDC_PROT2	-	-	TST_PROT1	CDC_xPROT1	-	-	(84h)
Description	F0	F1	F2	F3	Description								
	00	-	-	-	Command2 disable \ Gamma Command disable \ Test Command disable \ CDC Command disable \ GIP Command disable								
	02	-	-	-	Gamma enable								
	01	01	-	-	Command2 page enable								
	08	-	08	-	Test Command page enable								
	80	-	40	-	CDC Command page enable								
	10	-	-	10	GIP Command page enable								

	⌚: Don't care.												
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>84h</td> </tr> <tr> <td>S/W Reset</td> <td>84h</td> </tr> <tr> <td>H/W Reset</td> <td>84h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	84h	S/W Reset	84h	H/W Reset	84h				
Status	Default Value												
Power On Sequence	84h												
S/W Reset	84h												
H/W Reset	84h												

CSC4 (F3h): Command Set Ctrl 4

F3H	Command Set Ctrl 4												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CK	0	↑	1	-	1	1	1	1	0	0	1	1	(F3h)
parameter	1	↑	1	-	-	-	-	GIP_PROT2	-	-	-	GIP_xPROT1	(01h)
Description	F0	F1	F2	F3	Description								
	00	-	-	-	Command2 disable · Gamma Command disable · Test Command disable · CDC Command disable · GIP Command disable								
	02	-	-	-	Gamma enable								
	01	01	-	-	Command2 page enable								
	08	-	08	-	Test Command page enable								
	80	-	40	-	CDC Command page enable								
10	-	-	10	GIP Command page enable									
⌚: Don't care.													

Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h				
	Status	Default Value												
	Power On Sequence	01h												
	S/W Reset	01h												
H/W Reset	01h													

SPIOR (F4h): SPI Others Read

F4H	SPIOR (SPI Others Read)													
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
SPIOR	0	↑	1	-	1	1	1	1	0	1	0	0	(F4h)	
Parameter	No Parameter												-	
Description	<p>- SPI read enable/disable for command table 2</p> <p>Example :</p> <p>a.) Write Cmd 0xF4 (Enable) -> Read Cmd 1st -> Write Cmd 0xF4 (Disable) · Write Cmd 0xF4 (Enable) -> Read Cmd 2nd -> Write Cmd 0xF4 (Disable) · · ·</p> <p>b.) Write Cmd 0xF4 (Enable) -> Read Cmd 1st -> Read Cmd 2nd -> Write Cmd 0xF4 (Disable)</p> <p>“-“ Don't care</p>													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
	Status	Default Value												
	Power On Sequence	N/A												
	S/W Reset	N/A												
H/W Reset	N/A													

13.2 Command Table 1

COMMAND Table 1															
Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function	
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation	
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software Reset	
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID	
	1	1	↑		-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		-	ID1.6-0									ID1 read
	1	1	↑		-	ID2.6-0									ID2 read
	1	1	↑		-	ID3.6-0									ID3 read
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status	
	1	1	↑		-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		BSTON	MY	MX	MV	ML	RGB	MH	HSD			
	1	1	↑		-	IFPF.2-0				IDMON	-	SLOUT	NORON		
	1	1	↑		VSSON	-	INVON	-	-	DISON	TEON	-			
	1	1	↑		-	-	TELOM	-	-	-	-	-	-		
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power Mode	
	1	1	↑		-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		BSTON	IDMON	-	SLPOUT	NORON	DISON	-	-			
RDD MADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display MADCTL	
	1	1	↑		-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		MY	MX	MV	ML	BGR	MH	HSD	-			

COMMAND Table 1

Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
RDD COLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel Format
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	-	VIPF.2-0			-	IFPF.2-0				
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image Mode
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	VSSON	-	INVON	-	-	-	-	-		
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal Mode
	1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
	1	1	↑	-	TEON	TELOM	-	-	-	-	-	-		
RDBST	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read Busy Status
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	-	-	-	-	-	-	-	RDY		
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out
NOROFF	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Normal off
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Normal On
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off

COMMAND Table 1

Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function	
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on	
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off	
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on	
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column Address Set	
	1	↑	1		XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start:	
	1	↑	1		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		0≤XS≤X	
	1	↑	1		XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address start:	
	1	↑	1		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		S≤XE≤X	
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row Address Set	
	1	↑	1		YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start:	
	1	↑	1		YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		0≤YS≤Y	
	1	↑	1		YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address start:	
	1	↑	1		YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		S≤YE≤Y	
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory Write	
	1	↑	1		D1.7-0									Write data	
	1	↑	1		Dx.7-0										
	1	↑	1		Dn.7-0										
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory Read	
	1	1	↑		-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		D1.7-0									Read data	
	1	1	↑		Dx.7-0										
	1	1	↑		Dn.7-0										

COMMAND Table 1

Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function	
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Vertical Scrolling Definition	
	1	↑	1		-	-	-	-	-	-	-	-	TFA.8		
	1	↑	1		TFA.7-0										
	1	↑	1		-	-	-	-	-	-	-	-	VSA.8		
	1	↑	1		VSA.7-0										
	1	↑	1		-	-	-	-	-	-	-	-	BFA.8		
	1	↑	1		BFA.7-0										
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing Effect Line off	
TEON	0	↑	1	1	0	0	1	1	0	1	0	1	(35h)	Tearing Effect Line on	
	1	↑	1		-	-	-	-	-	-	-	-	TE_MD		
MADCTL	0	↑	1	1	0	0	1	1	0	1	1	0	(36h)	Memory Data Access Control	
	1	↑	1		MY	MX	MV	ML	RGB	MH	HSD	-			
VSCRSADD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Vertical Scrolling Start Address	
	1	↑	1		-	-	-	-	-	-	-	-	VSP.8		
	1	↑	1		VSP.7-0										
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle Mode off	
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle Mode on	
COLMOD	0	↑	1	1	0	0	1	1	1	0	1	0	(3Ah)	Interface Pixel Format	
	1	↑	1		-	VIPF.2-0			-	IFPF.2-0					
RAMWRC	0	↑	1	-	0	0	1	1	1	1	0	0	(3Ch)	Memory Write Continue	
	1	↑	1		D1.7-0										
	1	↑	1		Dx.7-0										
	1	↑	1		Dn.7-0										

COMMAND Table 1

Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function	
RAMRDC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)	Memory Write Continue	
	1	1	↑		-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		D1.7-0										Read data
	1	1	↑		Dx.7-0										
	1	1	↑		Dn.7-0										
HSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(43h)	Horizontal Scrolling Definition	
	1	↑	1		-	-	-	-	-	-	-	-	LFA8		
	1	↑	1		LFA.7-0										
	1	↑	1		-	-	-	-	-	-	-	-	HSA8		
	1	↑	1		HSA.7-0										
	1	↑	1		-	-	-	-	-	-	-	-	RFA8		
	1	↑	1		RFA.7-0										
TESLWR	0	↑	1	2	0	1	0	0	0	1	0	0	(44h)	Write Tear Scan Line	
	1	↑	1		-	-	-	-	N.11-8						
	1	↑	1		N.7-0										
TESLRD	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)	Read Tear Scan Line	
	1	1	↑		-	-	-	-	N.11-8				(00h)		
	1	1	↑		N.7-0										(00h)
HSCRSADD	0	↑	1	-	0	1	0	0	0	1	1	1	(47h)	Horizontal Scrolling Start Address	
	1	↑	1		-	-	-	-	-	-	-	-	HSP.8		
	1	↑	1		HSP.7-0										
RAMCLACT	0	↑	1	-	0	1	0	0	1	1	0	0	(4Ch)	Memory Clear Act	
	1	↑	1		-	-	-	-	-	-	-	-	FILLEN		
RAMCLSETR	0	↑	1	-	0	1	0	0	1	1	0	1	(4Dh)	Memory Clear Set R	
	1	↑	1		R.5-0										
RAMCLSETG	0	↑	1	-	0	1	0	0	1	1	1	0	(4Eh)	Memory Clear Set G	
	1	↑	1		G.5-0										
RAMCLSETB	0	↑	1	-	0	1	0	0	1	1	1	1	(4Fh)	Memory	

COMMAND Table 1

Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function	
	1	↑	1		B.5-0							-	-		Clear Set G
CDCCTR	0	↑		-	0	1	0	1	0	0	0	0	(50h)	CDC Control	
	1	↑	1		CDC_EN	CDC_CO MP_EN	CDC_CO MP_M	CDC_SI DE_M	CDC_NO TCH1_EN	CDC_NO TCH2_EN	-	-			
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)	Write Display Brightness	
	1	↑	1		DBV.7-0										
RDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)	Read Display Brightness	
	1	1	↑		-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		DBV.7-0										
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)	Write CTRL Display	
	1	↑	1		-	-	-	-	-	BL	-	-			
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)	Read CTRL Display	
	1	1	↑		-	-	-	-	-	-	-	-	Dummy read		
	1	1	↑		-	-	-	-	-	BL	-	-			
CPRAMWR	0	↑	1	-	0	1	1	0	1	1	0	0	(6Ch)	Compress Memory Write	
	1	↑	1		Write data stream										
CPRAMWRC	0	↑	1	-	0	1	1	0	1	1	0	1	(6Dh)	Compress Continue Write	
	1	↑	1		Write data stream										
CPCTRL	0	↑	1	-	0	1	1	0	1	1	1	1	(6Fh)	Compress CTRL	
	1	↑	1		GCOMPR_C262	-	-	GCOMPR_EN	-	-	-	RDY			
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1	
	1	1	↑		-	-	-	-	-	-	-	-	Dummy read		
	1	1	↑		-	-	ID1.6-0								

COMMAND Table 1

Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function	
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2	
	1	1	↑		-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		-	ID2.6-0									
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3	
	1	1	↑		-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		-	ID3.6-0									

NOP (00h)

00H	NOP (No Operation)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-
Description	This command is empty command. "-" Don't care												
Restriction													
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
Default	Status						Default Value						
	Power On Sequence						N/A						
	S/W Reset						N/A						
	H/W Reset						N/A						
Flow Chart													

SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-
Description	<p>"-" Don't care</p> <p>- When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values.</p> <p>- Frame memory contents are unaffected by this command.</p>												
Restriction	<p>It will be necessary to wait 5msec before sending new command following software reset.</p> <p>The display module loads all display suppliers' factory default values to the registers during this 5msec.</p> <p>If software reset is sent during sleep in mode, it will be necessary to wait 120msec before sending sleep out command.</p> <p>Software reset command cannot be sent during sleep out sequence.</p>												
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						

	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	N/A
	S/W Reset	N/A
	H/W Reset	N/A
Flow Chart	<pre> graph TD A[SWRESET] --> B([Display whole blank screen]) B --> C{{Set Commands to S/W Default Value}} C --> D([Sleep In Mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Trapezoid Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Rounded rectangle Sequential transfer: Wavy bottom 	

RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	ID1.6-0								(7Fh)
3 rd parameter	1	1	↑	-	ID2.6-0								(7Fh)
4 th parameter	1	1	↑	-	ID3.6-0								(7Fh)
Description	<p>-This read byte returns 24-bit display identification information.</p> <p>-The 1st parameter is dummy data</p> <p>-The 2nd parameter (ID1.6-0): LCD module's manufacturer ID.</p> <p>-The 3rd parameter (ID2.6-0): LCD module/driver version ID</p> <p>-The 4th parameter (ID3.6-0): LCD module/driver ID.</p> <p>-Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.</p> <p>“-“ Don't care</p>												
Restriction													
Register availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In						Yes						
Default	Status			Default Value									
				ID1	ID2	ID3							
	Power On Sequence			See description	See description	See description							
	S/W Reset			See description	See description	See description							
H/W Reset			See description	See description	See description								

RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	HSD	(00h)
3 rd parameter	1	1	↑	-	-	IFPF.2-0			IDMON	-	SLOUT	NORON	(61h)

4 th parameter	1	1	↑	-	VSSON	-	INVON	-	-	DISON	TEON	-	(00h)
5 th parameter	1	1	↑	-	-	-	TELOM	-	-	-	-	-	(00h)
Description	This command indicates the current status of the display as described in the table below:												
	Bit	Description											Value
	BSTON	Booster Voltage Status											'1' =Booster on, '0' =Booster off
	MY	Row Address Order (MY)											'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
	MX	Column Address Order (MX)											'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='0')
	MV	Row/Column Exchange (MV)											'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0')
	ML	Scan Address Order (ML)											'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1' =Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')
	RGB	RGB/ BGR Order (RGB)											'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
	MH	Horizontal Order											'0' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1')
	IFPF.2-0	Interface Color Pixel Format Definition											"101" = 16-bit / pixel, "110" = 18-bit / pixel, "111" = 16M truncated, others are not defined.
	IDMON	Idle Mode On/Off											'1' = On, "0" = Off
	SLPOUT	Sleep In/Out											'1' = Out, "0" = In
	NORON	Display Normal Mode On/Off											'1' = Normal Display,
	INVON	Inversion Status											'1' = On, "0" = Off
	DISON	Display On/Off											'1' = On, "0" = Off
TEON	Tearing effect line on/off											'1' = On, "0" = Off	
TELOM	Tearing effect line mode											'0' = mode1, '1' = mode2	
“-“ Don't care													

RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	-	(0Ah)

1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	BSTON	IDMON	-	SLPOUT	NORON	DISON	-	-	(08h)
Description	This command indicates the current status of the display as described in the table below:												
	Bit	Description										Value	
	BSTON	Booster Voltage Status										'1' =Booster on, '0' =Booster off	
	IDMON	Idle mode on/off										'1' = Idle Mode On, '0' = Idle Mode Off	
	PTLON	Partial mode on/off										'1' =Partial mode on, '0' =Partial mode off,	
	SLPOUT	Sleep in/out										'1' =Sleep out, '0' =Sleep in,	
	NORON	Display normal mode on/off										'1' = Normal display, '0' = Partial display,	
DISON	Display on/off										'1' =Display on, '0' =Display off,		
“-“ Don't care													
Register availability	Status					Availability							
	Normal Mode On, Idle Mode Off, Sleep Out					Yes							
	Normal Mode On, Idle Mode On, Sleep Out					Yes							
	Partial Mode On, Idle Mode Off, Sleep Out					Yes							
	Partial Mode On, Idle Mode On, Sleep Out					Yes							
	Sleep In					Yes							
Default	Status										Default Value (D7 to D0)		
	Power On Sequence										0000-1000(08h)		
	S/W Reset										0000-1000(08h)		
	H/W Reset										0000-1000(08h)		

RDDMADCTL (0Bh): Read Display MADCTL

0Bh	RDDMADCTL (Read Display MADCTL)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	MY	MX	MV	ML	RGB	MH	HSD	-	(00h)
Description	This command indicates the current status of the display as described in the table below:												
	Bit	Description										Value	

	MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')
	MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='1')
	MV	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0')
	ML	Scan Address Order (ML)	'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')
	RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')
	MH	Horizontal Order	'0' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1')
"- " Don't care			
Restriction	There is one dummy parameter when using Parallel interface.		
Register availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
Sleep In		Yes	
Default	Status		Default Value (D7 to D0)
	Power On Sequence		0000-0000 (00h)
	S/W Reset		No change
	H/W Reset		0000-0000 (00h)

RDDCOLMOD (0Ch): Read Display Pixel Format

0Ch	RDDCOLMOD (Read Display Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	-	VIPF.2-0			-	IFPF.2-0			(66h)
Description	This command indicates the current status of the display as described in the table below:												
	Bit		Description								Value		
	D7		-								Set to '0'		
	VIPF.2-0		RGB interface color format								'101' = 16 bit/pixel '110' = 18 bit/pixel		
	D3		-								Set to '0'		
	IFPF.2-0		Control interface color format								'101' = 16 bit/pixel '110' = 18 bit/pixel		
“-“ Don't care													
Restriction	There is one dummy parameter when using Parallel interface.												
Register availability	Status					Availability							
	Normal Mode On, Idle Mode Off, Sleep Out					Yes							
	Normal Mode On, Idle Mode On, Sleep Out					Yes							
	Partial Mode On, Idle Mode Off, Sleep Out					Yes							
	Partial Mode On, Idle Mode On, Sleep Out					Yes							
	Sleep In					Yes							
Default	Status					Default Value							
	Power On Sequence					0000-0110 (18 bit/pixel)							
	S/W Reset					No change							
	H/W Reset					0000-0110 (18 bit/pixel)							

RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (Read Display Image Mode)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	VSSON	-	INVON	-	-	-	-	-	(00h)
Description	This command indicates the current status of the display as described in the table below: -VSSON: Vertical scrolling on/off -INVON: Inversion on/off Others are no define and invalid "-" Don't care												
Restriction	There is one dummy parameter when using Parallel interface.												
Register availability	Status					Availability							
	Normal Mode On, Idle Mode Off, Sleep Out					Yes							
	Normal Mode On, Idle Mode On, Sleep Out					Yes							
	Partial Mode On, Idle Mode Off, Sleep Out					Yes							
	Partial Mode On, Idle Mode On, Sleep Out					Yes							
	Sleep In					Yes							
Default	Status					Default Value							
	Power On Sequence					0000-0000							
	S/W Reset					0000-0000							
	H/W Reset					0000-0000							

RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (Read Display Signal Status)																					
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)									
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-									
2 nd parameter	1	1	↑	-	TEON	TELOM	-	-	-	-	-	-	(00h)									
Description	This command indicates the current status of the display as described in the table below: <table border="1" style="margin: 10px auto;"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>TEON</td> <td>Tearing effect line on/off</td> <td>'1' = ON, '0' = OFF,</td> </tr> <tr> <td>TELOM</td> <td>Tearing effect line mode</td> <td>'1' = mode2, '0' = mode1,</td> </tr> </tbody> </table> "-" Don't care													Bit	Description	Value	TEON	Tearing effect line on/off	'1' = ON, '0' = OFF,	TELOM	Tearing effect line mode	'1' = mode2, '0' = mode1,
Bit	Description	Value																				
TEON	Tearing effect line on/off	'1' = ON, '0' = OFF,																				
TELOM	Tearing effect line mode	'1' = mode2, '0' = mode1,																				

Restriction	There is one dummy parameter when using Parallel interface.		
Register availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes
Default	Status		Default Value
	Power On Sequence		0000-0000
	S/W Reset		0000-0000
	H/W Reset		0000-0000

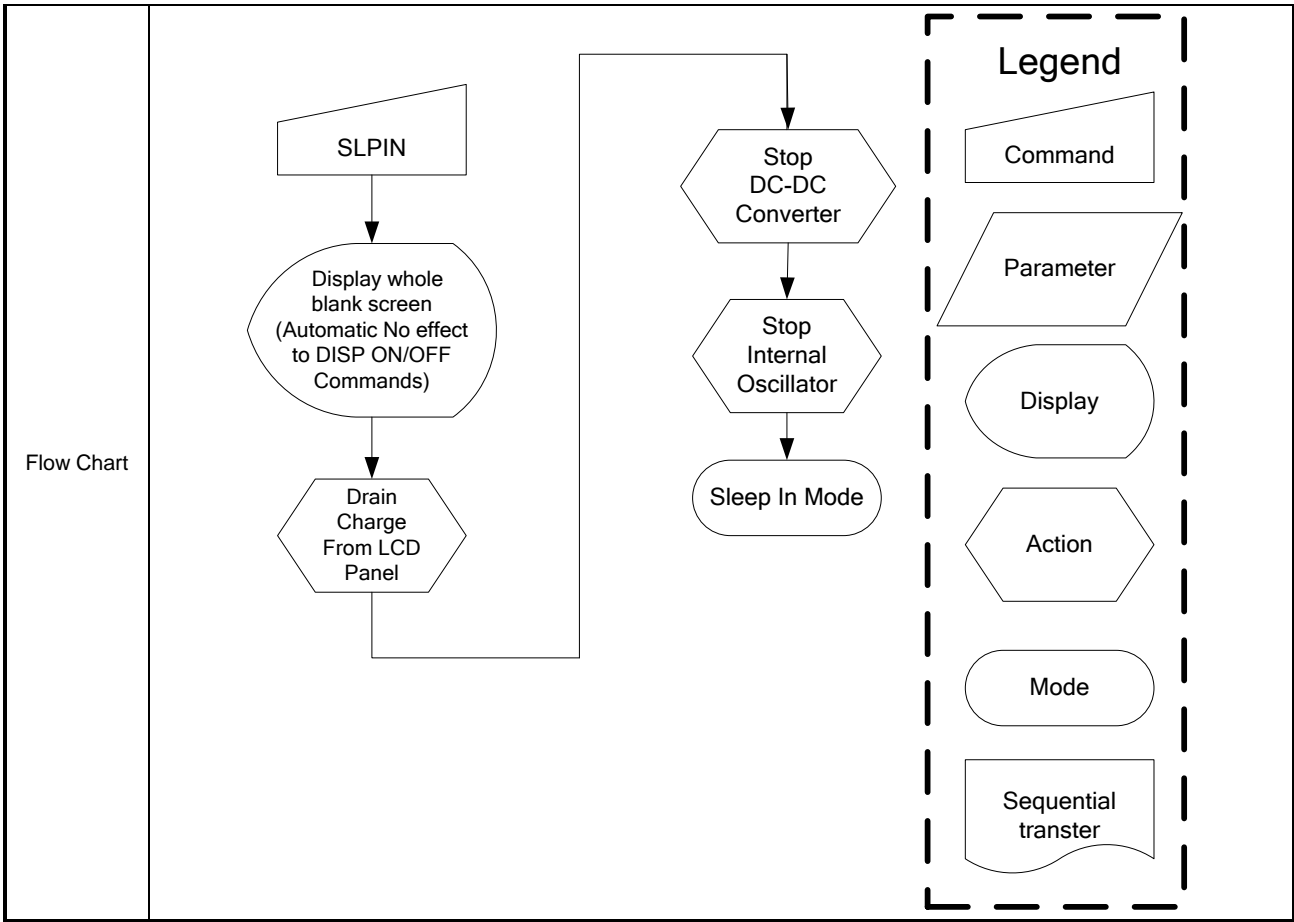
RDBST (0Fh): Read Busy Status

0FH	RDBST (Read Busy Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDBST	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	-	-	-	-	-	-	-	RDY	(00h)
Description	<p>This command indicates the current status of the display self-diagnostic result after sleep out command as described below:</p> <p>-CSCMP: Checksum comparison: '0' checksum the same; '1': checksum not the same.</p> <p>“-” Don't care</p>												
Restriction	There is one dummy parameter when using Parallel interface.												
Register availability	Status		Availability										
	Normal Mode On, Idle Mode Off, Sleep Out		Yes										
	Normal Mode On, Idle Mode On, Sleep Out		Yes										
	Partial Mode On, Idle Mode Off, Sleep Out		Yes										
	Partial Mode On, Idle Mode On, Sleep Out		Yes										
	Sleep In		Yes										
Default	Status		Default Value										
	Power On Sequence		0000-0000										
	S/W Reset		0000-0000										
	H/W Reset		0000-0000										

SLPIN (10h): Sleep in

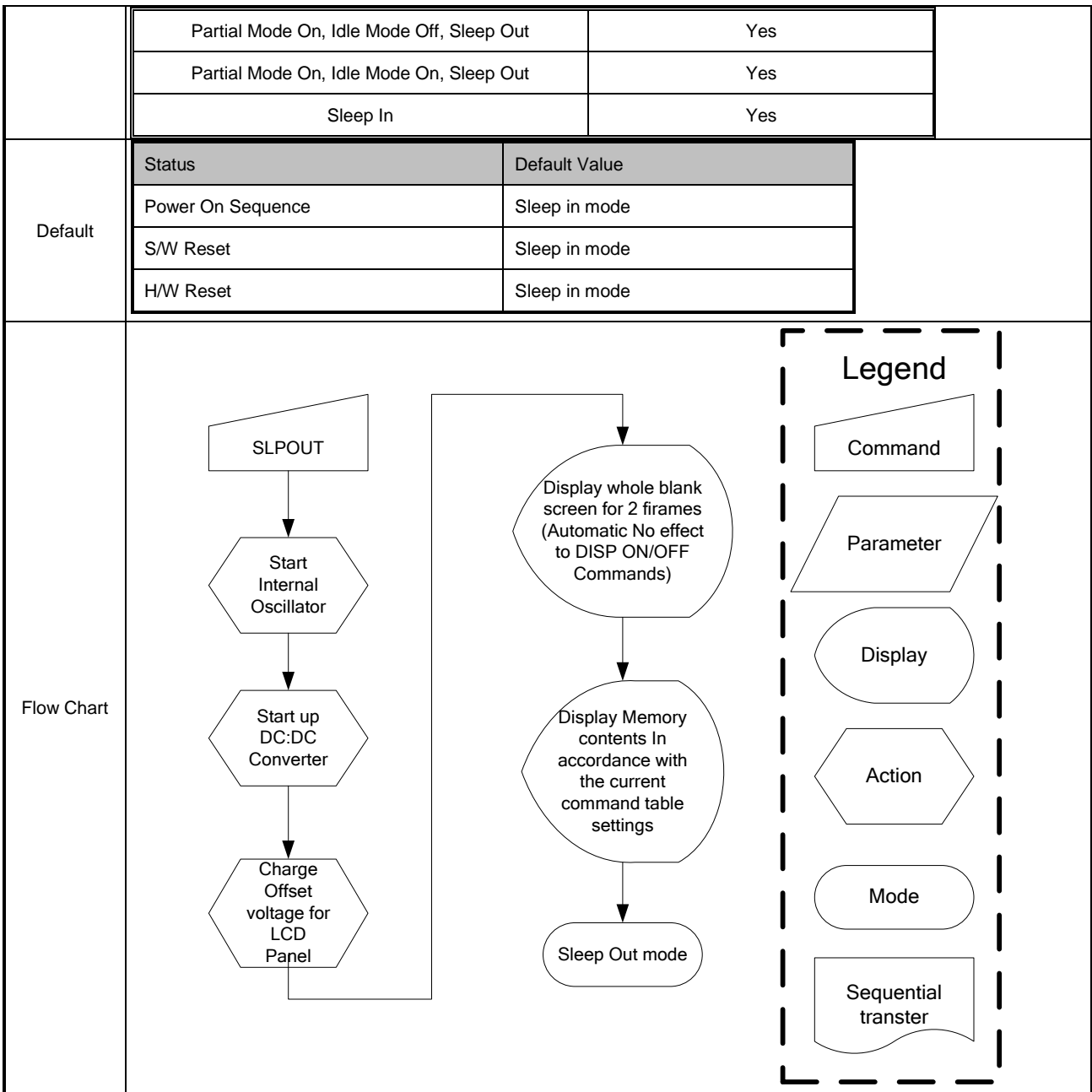
10H	SLPIN (Sleep In)
-----	------------------

Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)												
parameter	No Parameter																								
Description	<p>-This command causes the LCD module to enter the minimum power consumption mode.</p> <p>-In this mode the DC/DC converter is stopped, internal oscillator is stopped, and panel scanning is stopped.</p> <p>-MCU interface and memory are still working and the memory keeps its contents.</p> <p>-Dimming function does not work when there is changing mode from Sleep OUT to Sleep IN.</p> <p>“-“ Don't care</p>																								
Restriction	<p>-This command has no effect when module is already in sleep in mode. Sleep in mode can only be left by the sleep out command (11h).</p> <p>-It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize.</p> <p>-It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.</p>																								
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep in mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep in mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep in mode</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Sleep in mode	S/W Reset	Sleep in mode	H/W Reset	Sleep in mode				
Status	Default Value																								
Power On Sequence	Sleep in mode																								
S/W Reset	Sleep in mode																								
H/W Reset	Sleep in mode																								



SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)												HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)
parameter	No Parameter												
Description	-This command turn off sleep mode. -In this mode the DC/DC converter is enabled, internal display oscillator is started, and panel scanning is started.												
Restriction	-This command has no effect when module is already in sleep out mode. Sleep out mode can only be left by the sleep in command (10h). -It will be necessary to wait 5msec before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. -It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command. -The display module runs the self-diagnostic functions after this command is received.												
Register availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						



NOROFF (12h): Normal Off

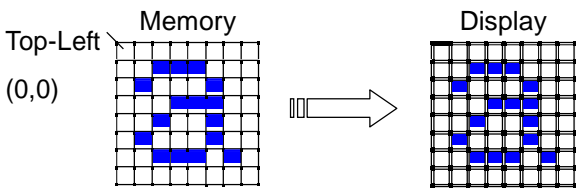
12H	NOROFF (Normal Off)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOROFF	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
parameter	No Parameter												
Description	-This command turns on Normal Off mode. The Normal Off mode will not enter Idle mode, but use Idle mode setting. -To leave Normal Off mode, the Normal On command (13h) should be written. "- Don't care												
Restriction	This command has no effect when Normal off mode is active.												
Register													

availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal display mode on</td> </tr> <tr> <td>S/W Reset</td> <td>Normal display mode on</td> </tr> <tr> <td>H/W Reset</td> <td>Normal display mode on</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Normal display mode on	S/W Reset	Normal display mode on	H/W Reset	Normal display mode on				
	Status	Default Value												
	Power On Sequence	Normal display mode on												
	S/W Reset	Normal display mode on												
H/W Reset	Normal display mode on													
Flow Chart														

NORON (13h): Normal On

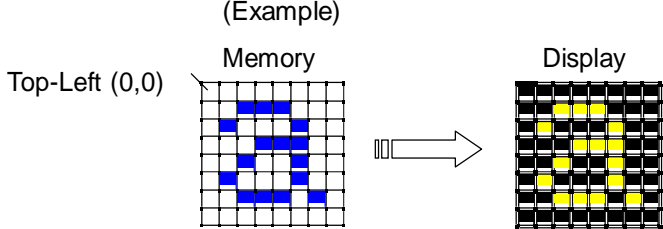
12H	NORON (Normal On)																								
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)												
parameter	No Parameter																								
Description	-This command turns the display to Normal On mode. -Normal display mode on means Normal off mode off. -Exit from NORON by the NOROFF command. "- " Don't care																								
Restriction	This command has no effect when Normal On mode is active.																								
Register availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal display mode on</td> </tr> <tr> <td>S/W Reset</td> <td>Normal display mode on</td> </tr> <tr> <td>H/W Reset</td> <td>Normal display mode on</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Normal display mode on	S/W Reset	Normal display mode on	H/W Reset	Normal display mode on				
Status	Default Value																								
Power On Sequence	Normal display mode on																								
S/W Reset	Normal display mode on																								
H/W Reset	Normal display mode on																								
Flow Chart																									

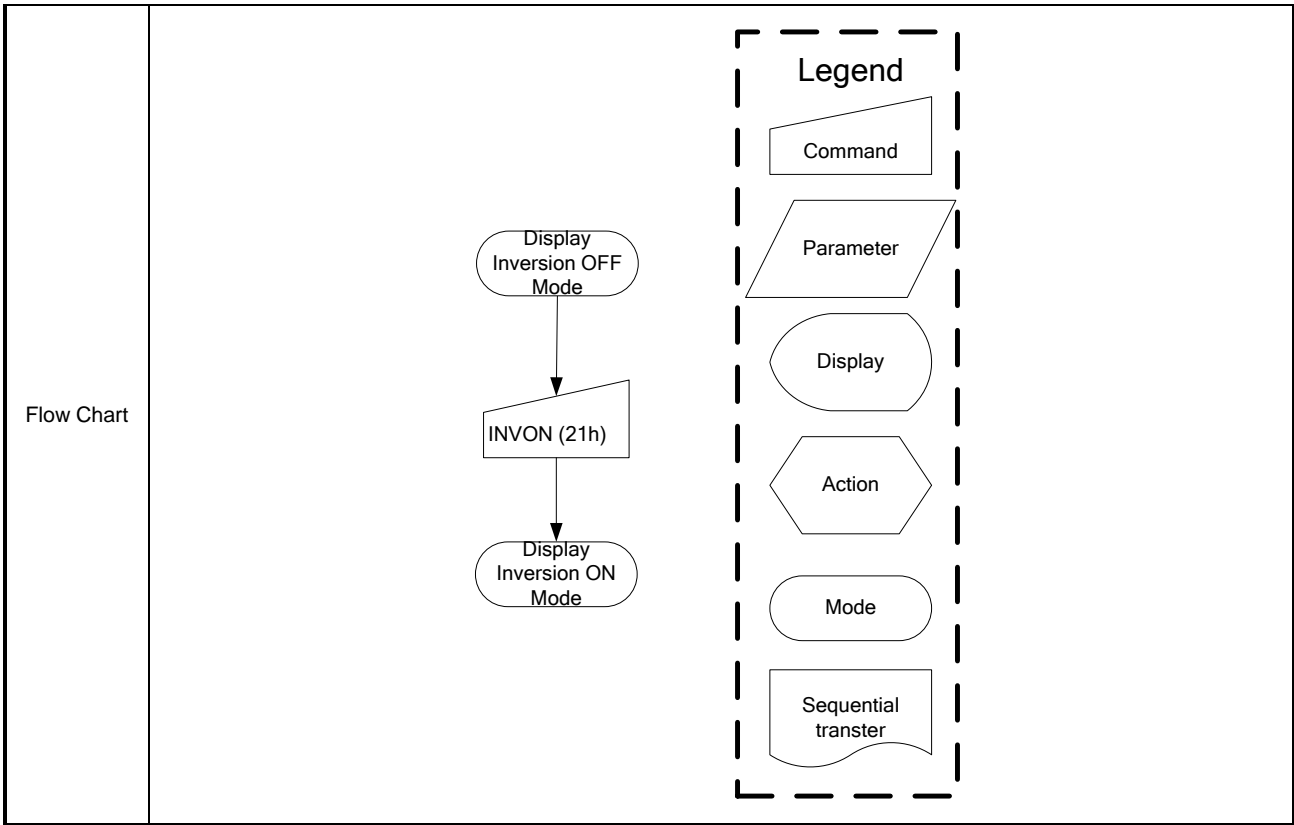
INVOFF (20h): Display Inversion Off

20H	INVOFF (Display Inversion Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)
parameter	No Parameter												
Description	-This command is used to recover from display inversion mode. "- " Don't care <div style="text-align: center; margin-top: 20px;"> (Example)  </div>												

Restriction	This command has no effect when module is already in inversion off mode.	
Register availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	Display inversion off
	S/W Reset	Display inversion off
	H/W Reset	Display inversion off
Flow Chart	<pre> graph TD A([Display Inversion On Mode]) --> B[/INVOFF (20h)/] B --> C([Display Inversion OFF Mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Rounded rectangle Sequential transfer: Rectangle with wavy bottom 	

INVON (21h): Display Inversion On

21H	INVON (Display Inversion On)												HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)
parameter	No Parameter												
Description	<p>-This command is used to recover from display inversion mode. "- Don't care</p> <p>(Example)</p> <p>Top-Left (0,0) </p>												
Restriction	This command has no effect when module is already in inversion on mode.												
Register availability	Status					Availability							
	Normal Mode On, Idle Mode Off, Sleep Out					Yes							
	Normal Mode On, Idle Mode On, Sleep Out					Yes							
	Partial Mode On, Idle Mode Off, Sleep Out					Yes							
	Partial Mode On, Idle Mode On, Sleep Out					Yes							
Default	Status					Default Value							
	Power On Sequence					Display inversion off							
	S/W Reset					Display inversion off							
	H/W Reset					Display inversion off							



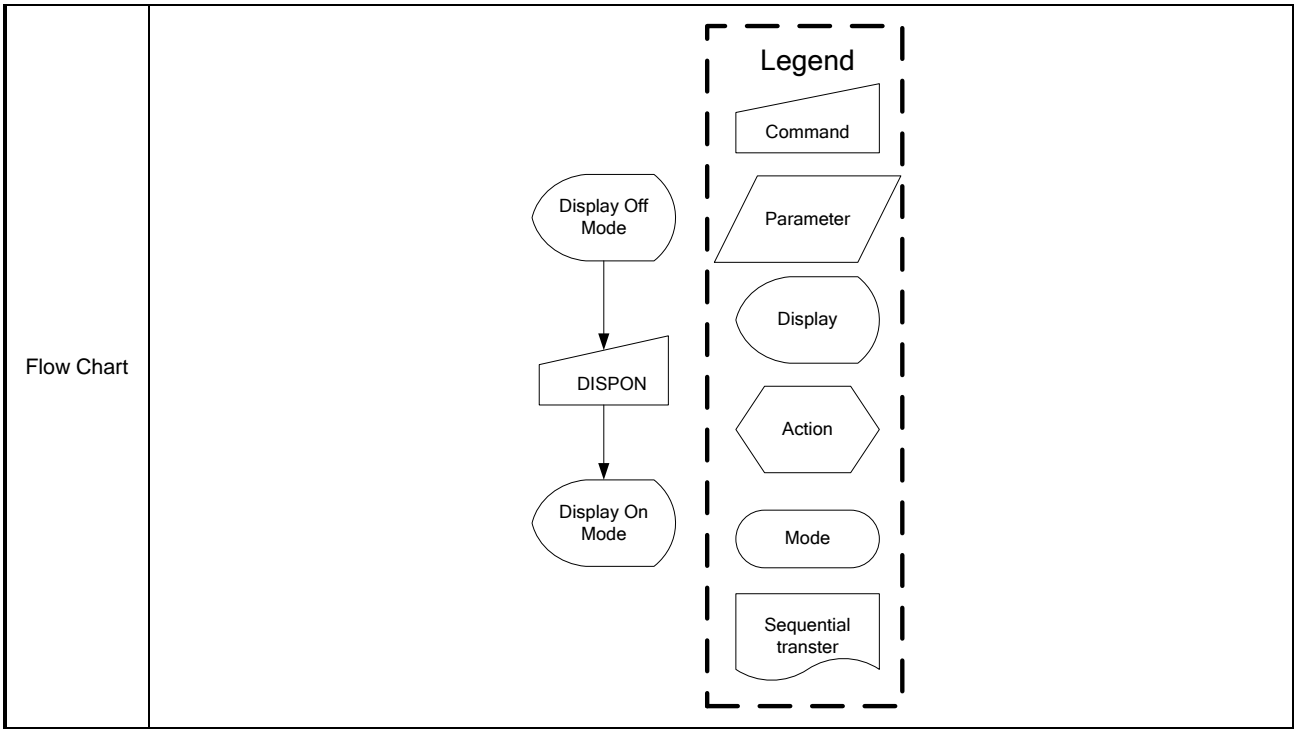
DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)												HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
parameter	No Parameter												
Description	<ul style="list-style-type: none"> - This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. - This command makes no change of contents of frame memory. - This command does not change any other status. - There will be no abnormal visible effect on the display. - Exit from this command by Display On (29h) <div style="text-align: center;"> <p>(Example)</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Memory</p> </div> <div style="font-size: 2em;">→</div> <div style="text-align: center;"> <p>Display</p> </div> </div> </div>												
Restriction	This command has no effect when module is already in display off mode.												

Register availability	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	
Default	Status		Default Value	
	Power On Sequence		Display off	
	S/W Reset		Display off	
	H/W Reset		Display off	
Flow Chart	<pre> graph TD A([Display On Mode]) --> B[/DISPOFF/] B --> C([Display Off Mode]) </pre>			
	<p>Legend</p> <ul style="list-style-type: none"> Command: trapezoid Parameter: parallelogram Display: rounded rectangle Action: hexagon Mode: rounded rectangle Sequential transfer: wavy-bottom rectangle 			

DISPON (29h): Display On

29H	DISPON (Display On)																								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
DISPO N	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)												
parameter	No Parameter																								
Description	<p>- This command is used to recover from DISPLAY OFF mode.</p> <p>- Output from the Frame Memory is enabled.</p> <p>- This command makes no change of contents of frame memory.</p> <p>- This command does not change any other status.</p> <div style="text-align: center;"> <p>(Example)</p> </div>																								
Restriction	This command has no effect when module is already in display on mode.																								
Register availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 50%;">Status</th> <th style="width: 50%;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off				
Status	Default Value																								
Power On Sequence	Display off																								
S/W Reset	Display off																								
H/W Reset	Display off																								



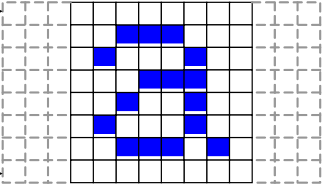
CASET (2Ah): Column Address Set

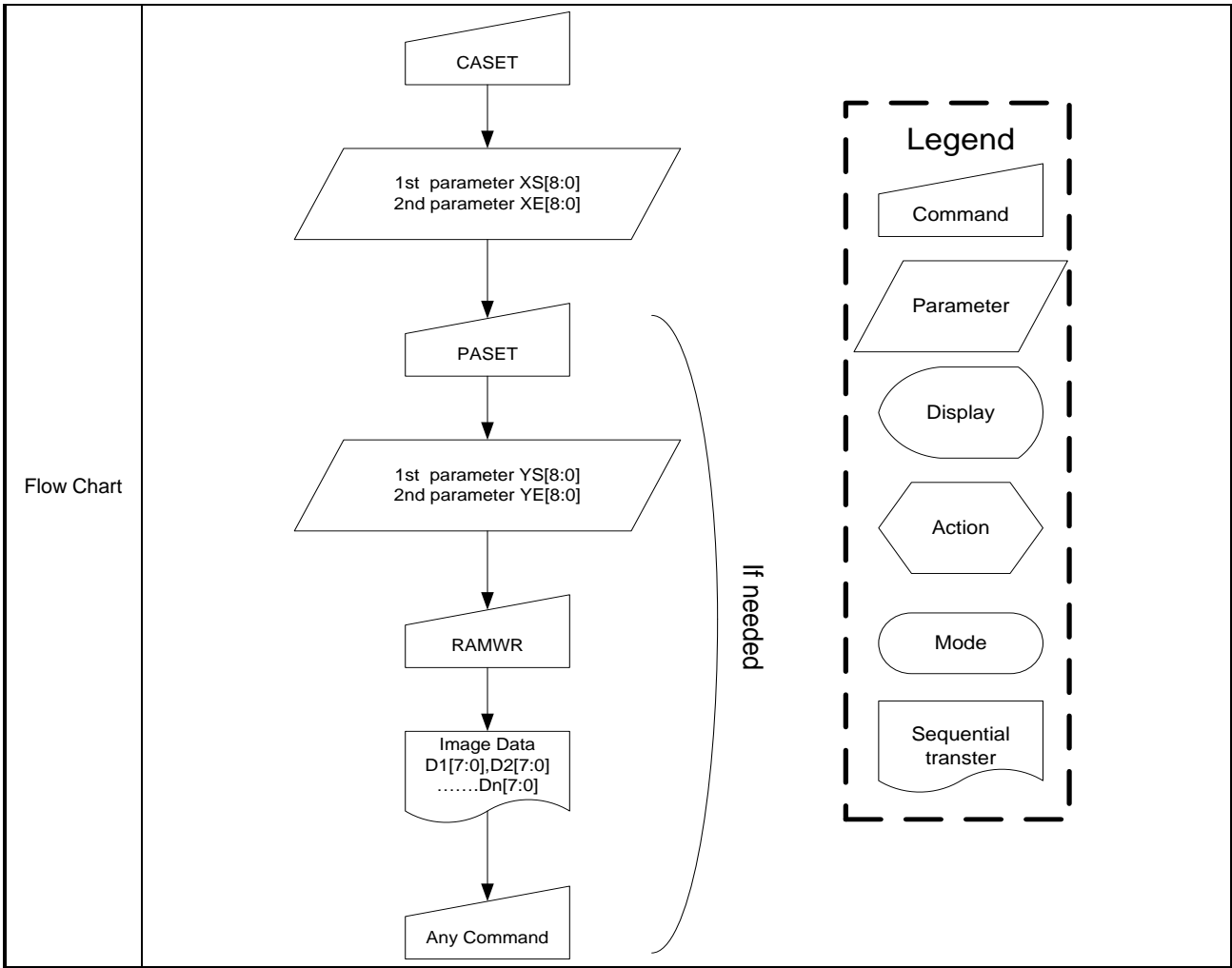
2AH	CASET (Column Address Set)												HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)
1 st parameter	1	↑	1	-	-	-	-	-	-	-	-	XS.8	(00h)
2 nd parameter	1	↑	1	-	XS.7-0							(00h)	
3 rd parameter	1	↑	1	-	-	-	-	-	-	-	-	XE.8	(01h)
4 th parameter	1	↑	1	-	XE.7-0							(67h)	
Description	<p>-The value of XS [8:0] and XE [8:0] are referred when RAMWR command comes.</p> <p>-Each value represents one column line in the Frame Memory.</p>												
Restriction	<p>XS [8:0] always must be equal to or less than XE [8:0]</p> <p>When XS [8:0] or XE [8:0] is greater than maximum address like below, data of out of range will be ignored.</p> <p>(Parameter range: 0 < XS [8:0] < XE [8:0] < 359 (0167h)): MV="0"</p> <p>(Parameter range: 0 < XS [8:0] < XE [8:0] < 389 (0185h)): MV="1"</p>												
Register availability	Status						Availability						

	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
	Power On Sequence	XS[8:0]=0x00	XE[8:0]=0167h
	S/W Reset	XS[8:0]=0x00	When MV=0: XE[8:0]=0167h, When MV=1: XE[8:0]=0185h
	H/W Reset	XS[8:0]=0x00	XE[8:0]=0167h
Flow Chart			

RASET (2Bh): Row Address Set

2BH	RASET (Row Address Set)												HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1 st parameter	1	↑	1	-	-	-	-	-	-	-	-	YS.8	(00h)

2 nd parameter	1	↑	1	-	YS.7-0								(00h)												
3 rd parameter	1	↑	1	-	-	-	-	-	-	-	-	YE.8	(01h)												
4 th parameter	1	↑	1	-	YE.7-0								(85h)												
Description	<p>-This command is used to define area of frame memory where MCU can access.</p> <p>-The value of YS [8:0] and YE [8:0] are referred when RAMWR command comes.</p> <p>-Each value represents one page line in the Frame Memory.</p> <p>YS[8:0] → </p>																								
Restriction	<p>YS [8:0] always must be equal to or less than YE [8:0]</p> <p>When YS [8:0] or YE [8:0] is greater than maximum address like below, data of out of range will be ignored.</p> <p>(Parameter range: 0 < YS [8:0] < YE [8:0] < 389 (0185h)): MV="0"</p> <p>(Parameter range: 0 < YS [8:0] < YE [8:0] < 359 (0167h)): MV="1"</p>																								
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>YS[8:0]=0000h</td> <td>YE[8:0]=0185h</td> </tr> <tr> <td>S/W Reset</td> <td>YS[8:0]=0000h</td> <td>When MV=0: YE[8:0]=0185h, When MV=1: YE[8:0]=0167h</td> </tr> <tr> <td>H/W Reset</td> <td>YS[8:0]=0000h</td> <td>YE[8:0]=0167h</td> </tr> </tbody> </table>													Status	Default Value		Power On Sequence	YS[8:0]=0000h	YE[8:0]=0185h	S/W Reset	YS[8:0]=0000h	When MV=0: YE[8:0]=0185h, When MV=1: YE[8:0]=0167h	H/W Reset	YS[8:0]=0000h	YE[8:0]=0167h
Status	Default Value																								
Power On Sequence	YS[8:0]=0000h	YE[8:0]=0185h																							
S/W Reset	YS[8:0]=0000h	When MV=0: YE[8:0]=0185h, When MV=1: YE[8:0]=0167h																							
H/W Reset	YS[8:0]=0000h	YE[8:0]=0167h																							



RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)
1 st parameter	1	↑	1	-	D1.7-0							-	
...	1	↑	1	-	Dx.7-0							-	
N parameter	1	↑	1	-	Dn.7-0							-	
Description	-This command is used to transfer data from MCU to frame memory. -When this command is accepted, the column register and the page register are reset to the start column/start page positions. -The start column/start page positions are different in accordance with MADCTL setting. -Sending any other command can stop frame write.												
Restriction	In all color modes, there is no restriction on length of parameters.												
Register availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						

	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	Contents of memory is set randomly
	S/W Reset	Contents of memory is not cleared
	H/W Reset	Contents of memory is not cleared
Flow Chart		

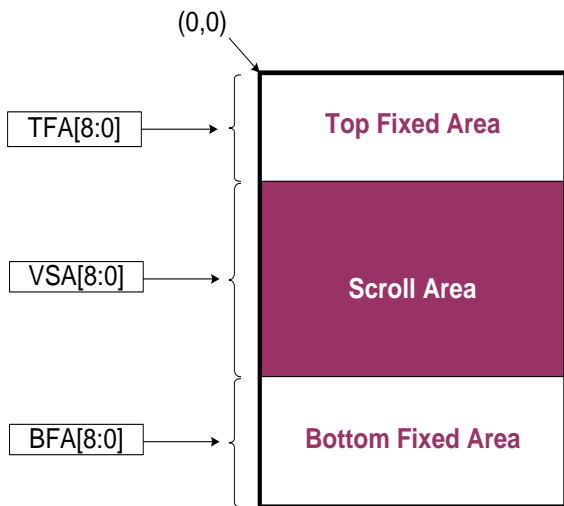
RAMRD (2Eh): Memory Read

2CH	RAMRD (Memory Read)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd parameter	1	1	↑	-	D1.7-0							-	
:	1	1	↑	:	:							:	
(N+1) th parameter	1	1	↑	-	Dn.7-0							-	
Description	-This command is used to transfer data from frame memory to MCU. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTL setting. -Then D[8:0] is read back from the frame memory and the column register and the row register incremented												

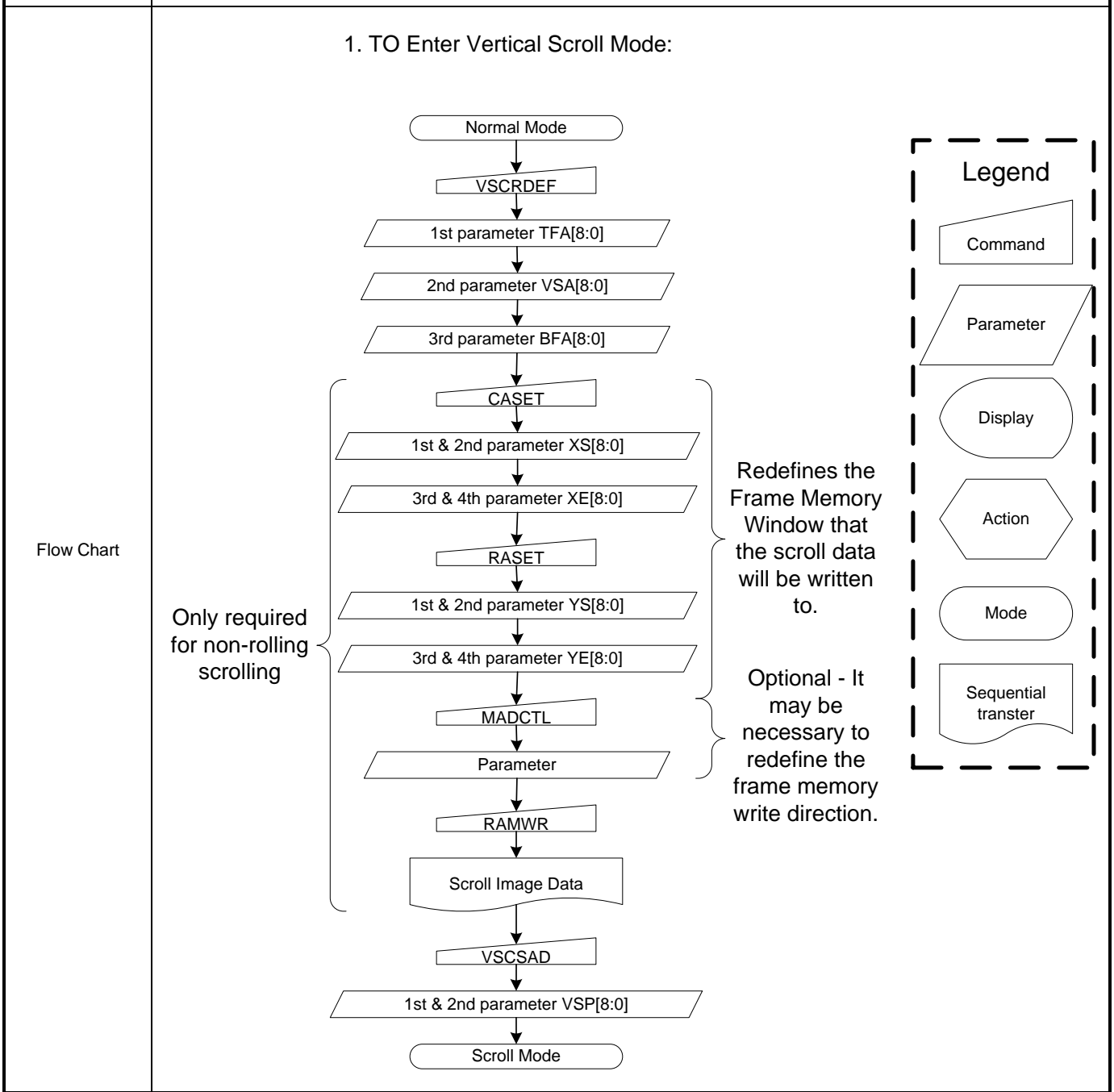
	<p>-Frame Read can be cancelled by sending any other command.</p> <p>-The data color coding is fixed to 18-bit in reading function. Please see section 9.8 "Data color coding" for color coding (18-bit cases), when there is used 8, 9 data lines for image data.</p> <p>Note1: The Command 3Ah should be set to 66h when reading pixel data from frame memory.</p>												
Restriction													
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value												
Power On Sequence	Contents of memory is set randomly												
S/W Reset	Contents of memory is not cleared												
H/W Reset	Contents of memory is not cleared												
Flow Chart													

VSCRDEF (33h): Vertical Scrolling Definition

33H	VSCRDEF (Vertical Scrolling Definition)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX

VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)												
1 st parameter	1	↑	1	-	-	-	-	-	-	-	-	TFA.8	(00h)												
2 nd parameter	1	↑	1	-	TFA.7-0							(00h)													
3 rd parameter	1	↑	1	-	-	-	-	-	-	-	-	VSA.8	(01h)												
4 th parameter	1	↑	1	-	VSA.7-0							(86h)													
5 th parameter	1	↑	1	-	-	-	-	-	-	-	-	BFA.8	(00h)												
6 th parameter	1	↑	1	-	BFA.7-0							(00h)													
Description	<p>-This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll</p> <p>-When MADCTL MV=0</p> <p>-The 1st & 2nd parameter TFA [8:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).</p> <p>-The 3rd & 4th parameter VSA [8:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area.</p> <p>-The 5th & 6th parameter BFA [8:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).</p> <p>TFA, VSA and BFA refer to the Frame Memory Line Pointer</p> 																								
Restriction	<p>The condition is $TFA+VSA+BFA = 390$, otherwise Scrolling mode is undefined.</p> <p>In Vertical Scrolling Mode, MADCTL parameter MV should be set to '0' – this only affects the Frame Memory write.</p>																								
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

Status	Default Value		
Power On Sequence	TFA[8:0] = 0000h	VSA[8:0] = 0186h	BFA[8:0] = 0000h
S/W Reset	TFA[8:0] = 0000h	VSA[8:0] = 0186h	BFA[8:0] = 0000h
H/W Reset	TFA[8:0] = 0000h	VSA[8:0] = 0186h	BFA[8:0] = 0000h



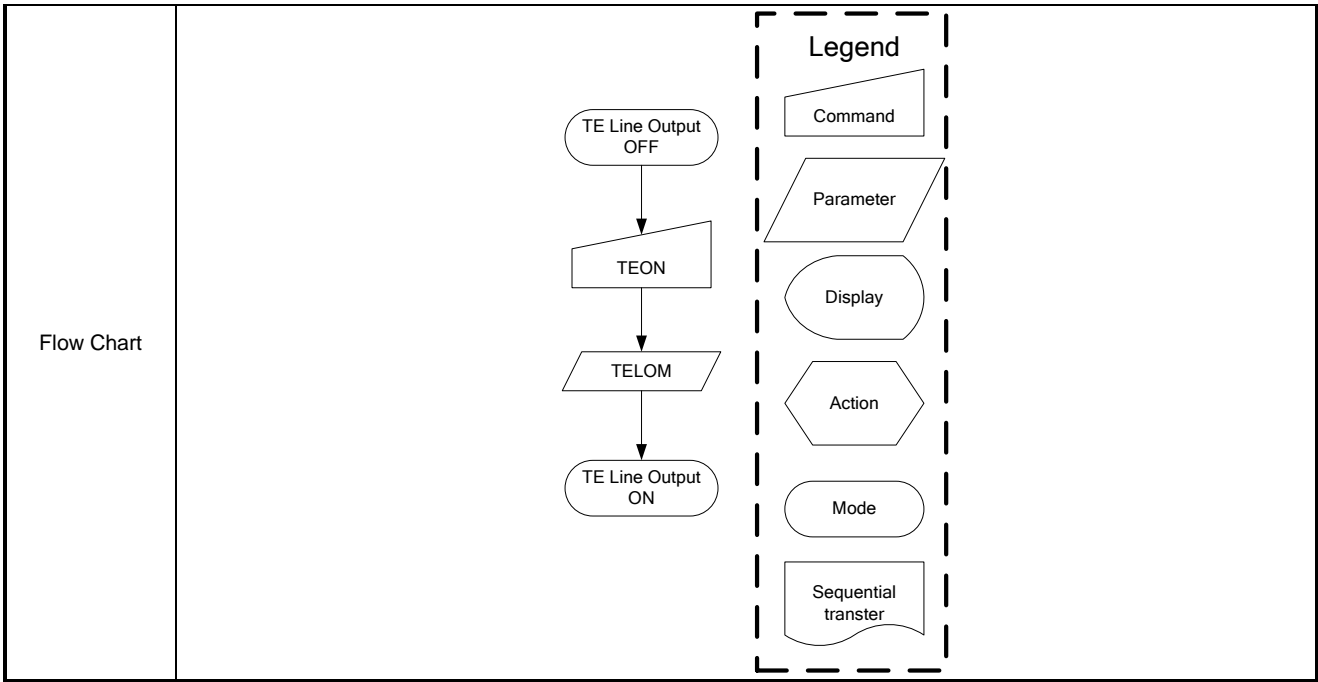
TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)

parameter	No Parameter	
Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.	
Restriction	This command has no effect when tearing effect output is already off..	
Register availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	Off
	S/W Reset	Off
	H/W Reset	Off
Flow Chart	<div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center; margin-right: 20px;"> <p>TE Line Output ON</p> <p>↓</p> <p>TEOFF</p> <p>↓</p> <p>TE Line Output OFF</p> </div> <div style="border: 1px dashed black; padding: 10px;"> <p>Legend</p> <p>▭ Command</p> <p>▱ Parameter</p> <p>○ Display</p> <p>⬡ Action</p> <p>⭕ Mode</p> <p>▭ Sequential transter</p> </div> </div>	

TEON (35h): Tearing Effect Line On

35H	TEON (Tearing Effect Line On)												HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
parameter	1	↑	1	-	0	0	0	0	0	0	0	TE_MD	(00h)
Description	<p>-This command is used to turn ON the Tearing Effect output signal from the TE signal line.</p> <p>-This output is not affected by changing MADCTL bit ML.</p> <p>-The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line:</p> <p>-When TEM = '0': The Tearing Effect output line consists of V-Blanking information only</p> <p>-When TEM = '1': The Tearing Effect output Line consists of both V-Blanking and H-Blanking information</p> <p>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</p>												
Restriction	This command has no effect when tearing effect output is already on.												
Register availability			Status					Availability					
			Normal Mode On, Idle Mode Off, Sleep Out					Yes					
			Normal Mode On, Idle Mode On, Sleep Out					Yes					
			Partial Mode On, Idle Mode Off, Sleep Out					Yes					
			Partial Mode On, Idle Mode On, Sleep Out					Yes					
			Sleep In					Yes					
Default	Status		Default Value										
	Power On Sequence		Off										
	S/W Reset		Off										
	H/W Reset		Off										



MADCTL (36h): Memory Data Access Control

36H	MADCTL (Memory Data Access Control)												HEX																								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																								
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)																								
parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	HSD	-	(00h)																								
Description	-This command defines read/ write scanning direction of frame memory.																																				
	<table border="1"> <thead> <tr> <th>Bit</th> <th>NAME</th> <th>DESCRIPTION</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>MY</td> <td>Page Address Order</td> </tr> <tr> <td>D6</td> <td>MX</td> <td>Column Address Order</td> </tr> <tr> <td>D5</td> <td>MV</td> <td>Page/Column Order</td> </tr> <tr> <td>D4</td> <td>ML</td> <td>Line Address Order</td> </tr> <tr> <td>D3</td> <td>RGB</td> <td>RGB/BGR Order</td> </tr> <tr> <td>D2</td> <td>MH</td> <td>Display Data Latch Order</td> </tr> <tr> <td>D1</td> <td>HSD</td> <td>Horizontal Scroll Address Order</td> </tr> </tbody> </table>													Bit	NAME	DESCRIPTION	D7	MY	Page Address Order	D6	MX	Column Address Order	D5	MV	Page/Column Order	D4	ML	Line Address Order	D3	RGB	RGB/BGR Order	D2	MH	Display Data Latch Order	D1	HSD	Horizontal Scroll Address Order
	Bit	NAME	DESCRIPTION																																		
	D7	MY	Page Address Order																																		
	D6	MX	Column Address Order																																		
	D5	MV	Page/Column Order																																		
	D4	ML	Line Address Order																																		
	D3	RGB	RGB/BGR Order																																		
	D2	MH	Display Data Latch Order																																		
	D1	HSD	Horizontal Scroll Address Order																																		
-Bit Assignment																																					
Bit D7- Page Address Order																																					
"0" = Top to Bottom (When MADCTL D7="0").																																					
"1" = Bottom to Top (When MADCTL D7="1").																																					
Bit D6- Column Address Order																																					
"0" = Left to Right (When MADCTL D6="0").																																					
"1" = Right to Left (When MADCTL D6="1").																																					
Bit D5- Page/Column Order																																					

"0" = Normal Mode (When MADCTL D5="0").

"1" = Reverse Mode (When MADCTL D5="1")

Note: Bits D7 to D5, also refer to section 8.12 Address Control

Bit D4- Line Address Order

"0" = LCD Refresh Top to Bottom (When MADCTL D4="0")

"1" = LCD Refresh Bottom to Top (When MADCTL D4="1")

Bit D3- RGB/BGR Order

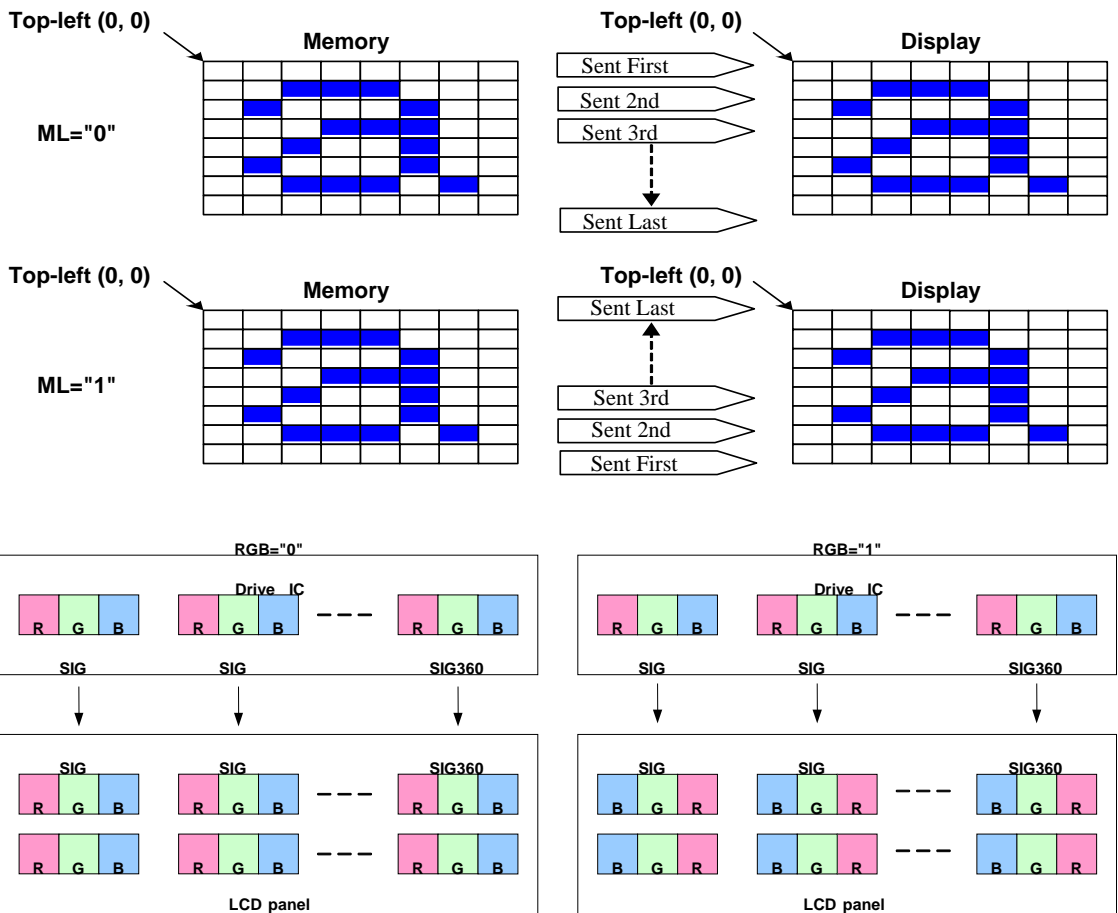
"0" = RGB (When MADCTL D3="0")

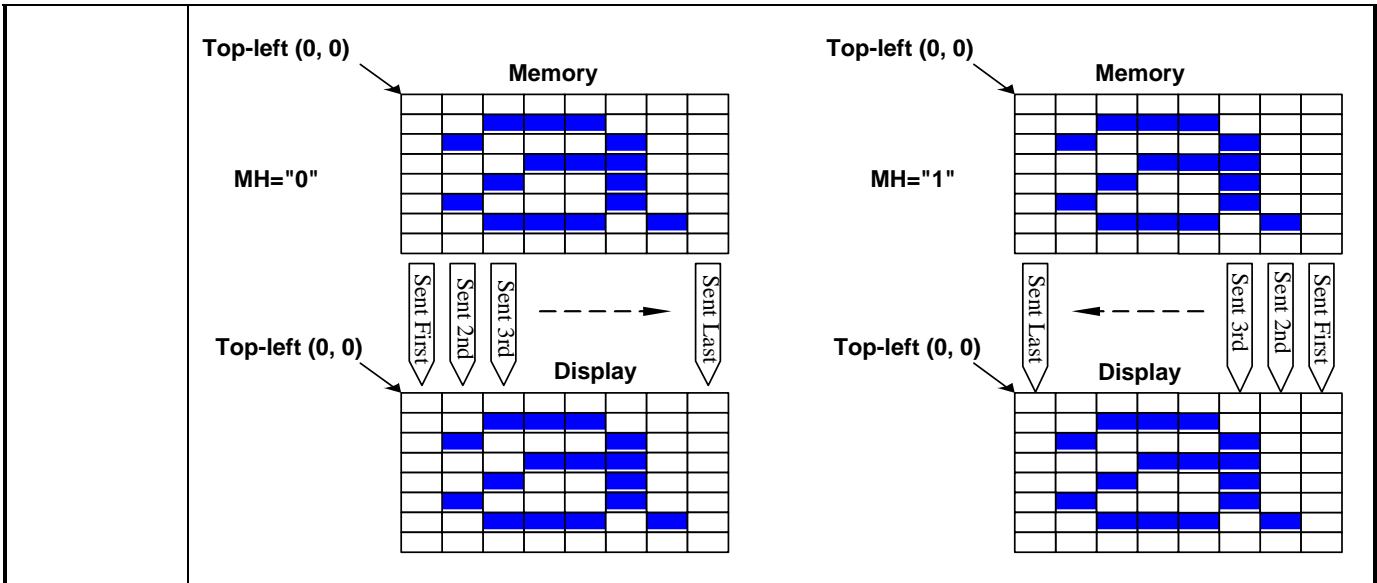
"1" = BGR (When MADCTL D3="1")

Bit D2- Display Data Latch Data Order

"0" = LCD Refresh Left to Right (When MADCTL D2="0")

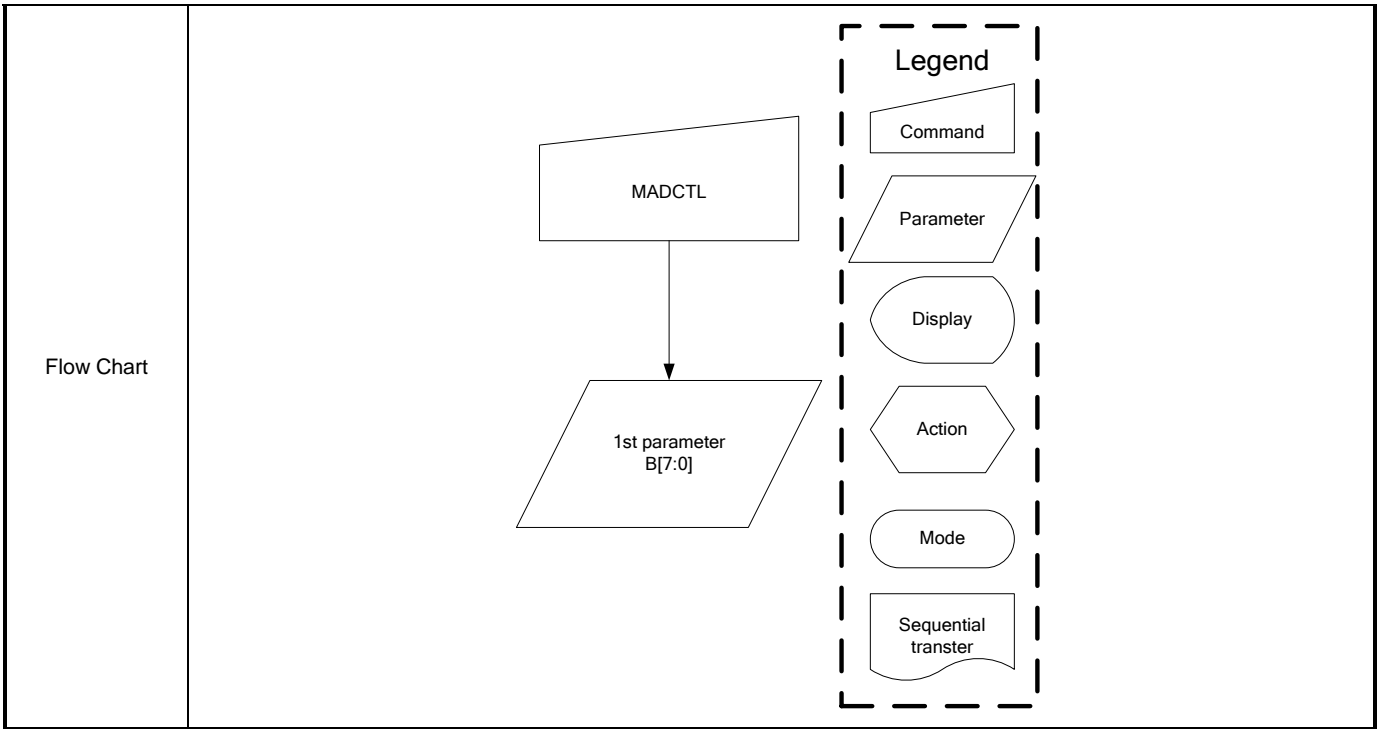
"1" = LCD Refresh Right to Left (When MADCTL D2="1")





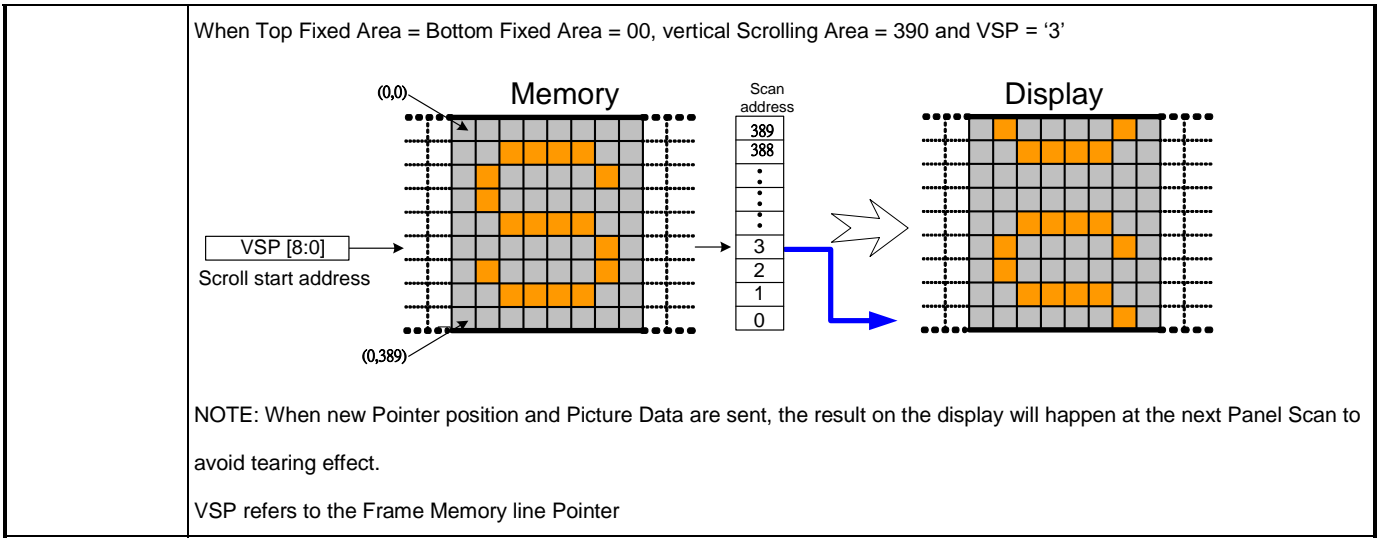
Register availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default Value
	Power On Sequence	0000h
	S/W Reset	No change
	H/W Reset	0000h



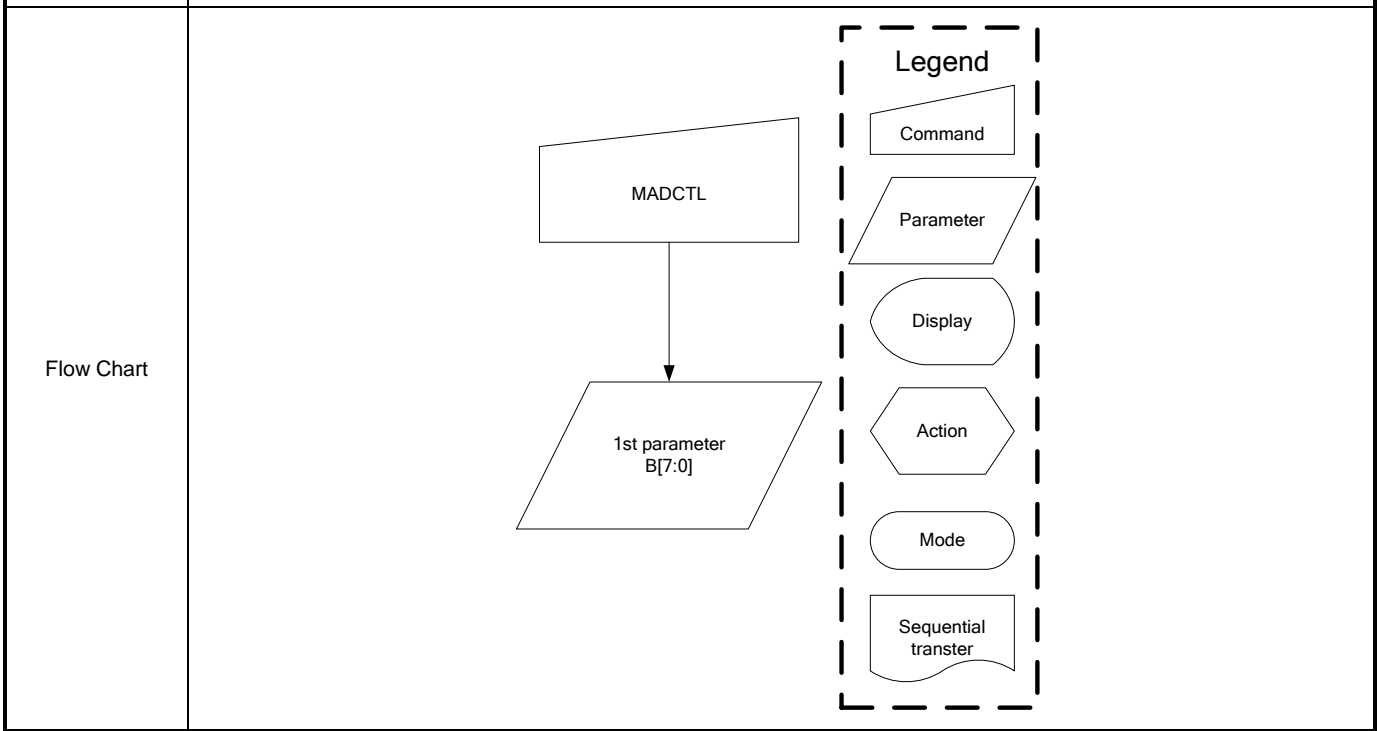
VSCSAD (37h): Vertical Scroll Start Address of RAM

37H	VSCSAD (Vertical Scroll Start Address of RAM)												HEX
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)
1 ST parameter	1	↑	1	-	-	-	-	-	-	-	-	VSP.8	(00h)
2 ND parameter	1	↑	1	-	VSP.7-0							(00h)	
Description	<p>-This command is used together with Vertical Scrolling Definition (33h).</p> <p>-These two commands describe the scrolling area and the scrolling mode.</p> <p>-The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:</p> <p>When ML=0</p> <p>Example:</p> <p>When Top Fixed Area = Bottom Fixed Area = 00, vertical Scrolling Area = 390 and VSP = '3'</p> <p>When ML=1</p> <p>Example:</p>												



Register availability Since the value of the vertical scrolling start address is absolute (with reference to the frame memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h)- otherwise undesirable image will be displayed on the panel)

Status	Default Value
Power On Sequence	0000h
S/W Reset	No change
H/W Reset	0000h



IDMOFF (38h): Idle Mode Off

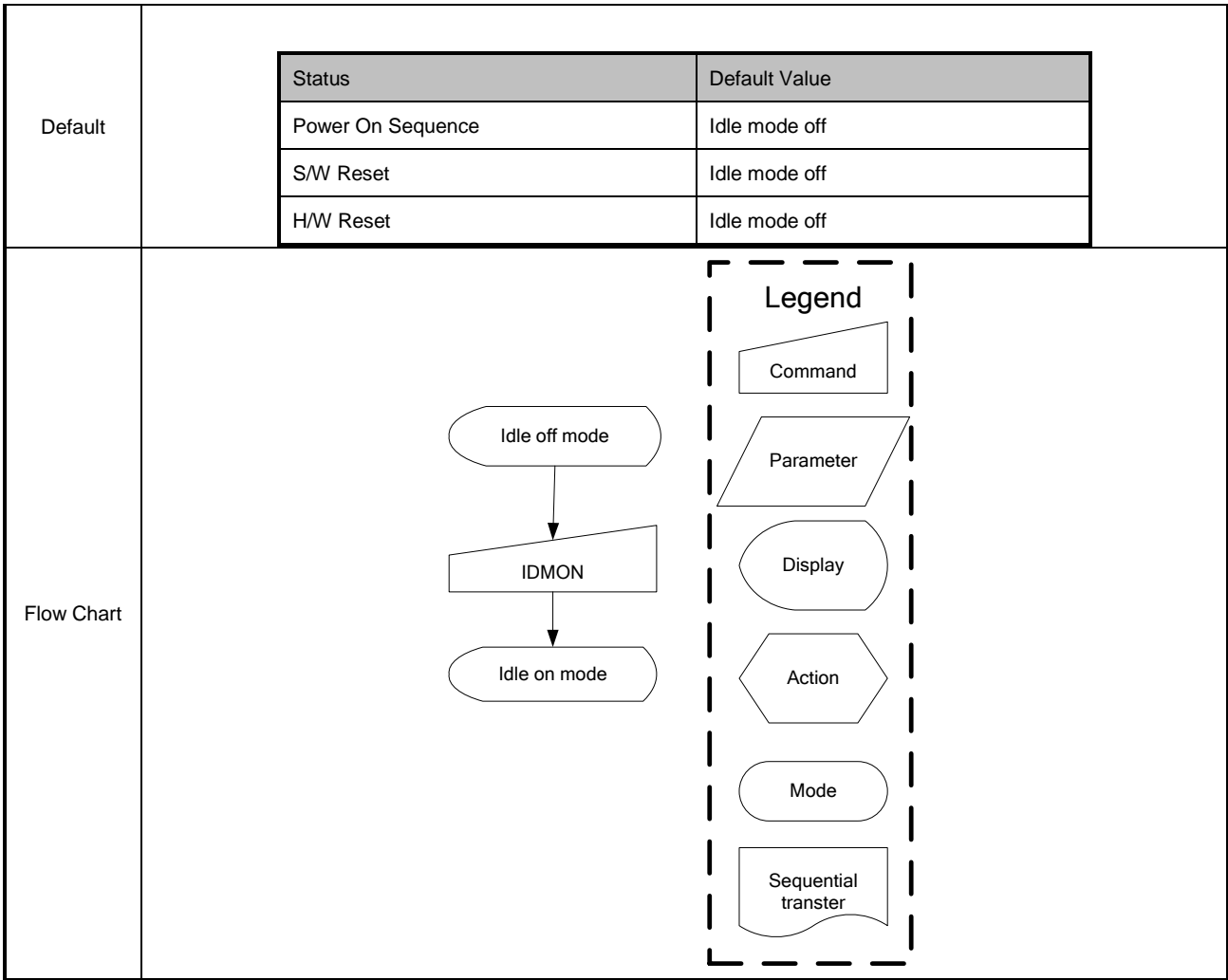
38H	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)

parameter	No Parameter												
Description	-This command is used to recover from Idle mode on. -In the idle off mode, 1. LCD can display 65k or 262k colors. 2. Normal frame frequency is applied.												
Restriction	This command has no effect when module is already in idle off mode												
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Idle mode off</td> </tr> <tr> <td>S/W Reset</td> <td>Idle mode off</td> </tr> <tr> <td>H/W Reset</td> <td>Idle mode off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Idle mode off	S/W Reset	Idle mode off	H/W Reset	Idle mode off				
Status	Default Value												
Power On Sequence	Idle mode off												
S/W Reset	Idle mode off												
H/W Reset	Idle mode off												
Flow Chart	<pre> graph TD A([Idle on mode]) --> B[/IDMOFF/] B --> C([Idle off mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Trapezoid Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Rounded rectangle Sequential transfer: Wavy rectangle 												

IDMON (39h): Idle Mode On

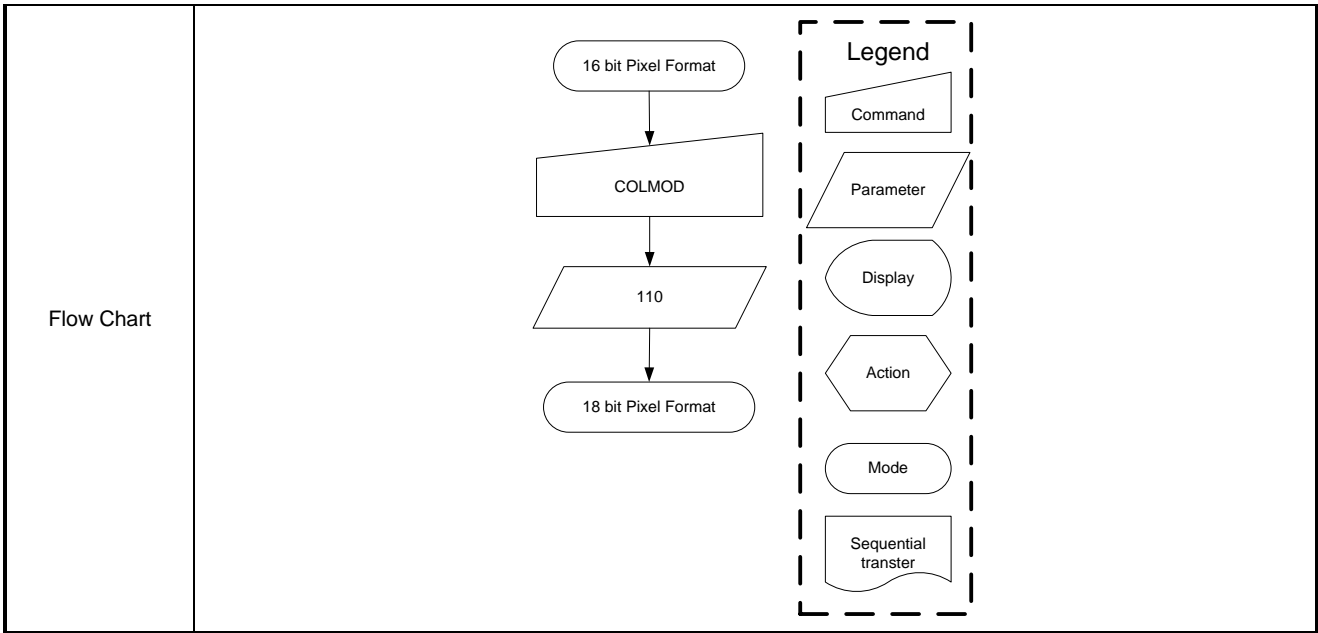
39H	IDMON (Idle Mode On)
-----	----------------------

Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)																																			
parameter	No Parameter																																															
Description	<p>-This command is used to enter into Idle mode on.</p> <p>-There will be no abnormal visible effect on the display mode change transition.</p> <p>-In the idle on mode,</p> <ol style="list-style-type: none"> Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed. 8-Color mode frame frequency is applied. Exit from IDMON by Idle Mode Off (38h) command 																																															
	<div style="text-align: center;"> <p>Top-Left (0,0) (Example) Memory Display</p> </div> <table border="1" style="margin: 10px auto; width: 80%;"> <thead> <tr> <th>Color</th> <th>R5 R4 R3 R2 R1 R0</th> <th>G5 G4 G3 G2 G1 G0</th> <th>B5 B4 B3 B4 B1 B0</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0xxxxx</td> <td>0xxxxx</td> <td>0xxxxx</td> </tr> <tr> <td>Blue</td> <td>0xxxxx</td> <td>0xxxxx</td> <td>1xxxxx</td> </tr> <tr> <td>Red</td> <td>1xxxxx</td> <td>0xxxxx</td> <td>0xxxxx</td> </tr> <tr> <td>Magenta</td> <td>1xxxxx</td> <td>0xxxxx</td> <td>1xxxxx</td> </tr> <tr> <td>Green</td> <td>0xxxxx</td> <td>1xxxxx</td> <td>0xxxxx</td> </tr> <tr> <td>Cyan</td> <td>0xxxxx</td> <td>1xxxxx</td> <td>1xxxxx</td> </tr> <tr> <td>Yellow</td> <td>1xxxxx</td> <td>1xxxxx</td> <td>0xxxxx</td> </tr> <tr> <td>White</td> <td>1xxxxx</td> <td>1xxxxx</td> <td>1xxxxx</td> </tr> </tbody> </table>													Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0	Black	0xxxxx	0xxxxx	0xxxxx	Blue	0xxxxx	0xxxxx	1xxxxx	Red	1xxxxx	0xxxxx	0xxxxx	Magenta	1xxxxx	0xxxxx	1xxxxx	Green	0xxxxx	1xxxxx	0xxxxx	Cyan	0xxxxx	1xxxxx	1xxxxx	Yellow	1xxxxx	1xxxxx	0xxxxx	White	1xxxxx	1xxxxx
Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0																																													
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Red	1xxxxx	0xxxxx	0xxxxx																																													
Magenta	1xxxxx	0xxxxx	1xxxxx																																													
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Yellow	1xxxxx	1xxxxx	0xxxxx																																													
White	1xxxxx	1xxxxx	1xxxxx																																													
Restriction	This command has no effect when module is already in idle off mode																																															
Register availability	<table border="1" style="margin: 10px auto; width: 80%;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																							
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MOLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (Interface Pixel Format)																											
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)															
Parameter	1	↑	1	-	-	VIPF.2-0			-	IFPF.2-0			(66h)															
Description	<p>This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:</p> <p>1st parameter:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>-</td> <td>Set to '0'</td> </tr> <tr> <td>VIPF.2-0</td> <td>RGB interface color format</td> <td>'101' = 65K of RGB interface '110' = 262K of RGB interface</td> </tr> <tr> <td>D3</td> <td>-</td> <td>Set to '0'</td> </tr> <tr> <td>IFPF.2-0</td> <td>Control interface color format</td> <td>'101' = 16bit/pixel '110' = 18bit/pixel</td> </tr> </tbody> </table> <p>Note1: In 16-bit/Pixel or 18-bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory. Note2: The Command 3Ah should be set at 55h when writing 16-bit/pixel data into frame memory, but 3Ah should be re-set to 66h when reading pixel data from frame memory.</p>													Bit	Name	Description	D7	-	Set to '0'	VIPF.2-0	RGB interface color format	'101' = 65K of RGB interface '110' = 262K of RGB interface	D3	-	Set to '0'	IFPF.2-0	Control interface color format	'101' = 16bit/pixel '110' = 18bit/pixel
	Bit	Name	Description																									
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	VIPF.2-0	RGB interface color format	'101' = 65K of RGB interface '110' = 262K of RGB interface																									
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IFPF.2-0	Control interface color format	'101' = 16bit/pixel '110' = 18bit/pixel																										
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
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Sleep In	Yes																											
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>18bit/pixel</td> </tr> <tr> <td>S/W Reset</td> <td>No change</td> </tr> <tr> <td>H/W Reset</td> <td>18bit/pixel</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	18bit/pixel	S/W Reset	No change	H/W Reset	18bit/pixel							
	Status	Default Value																										
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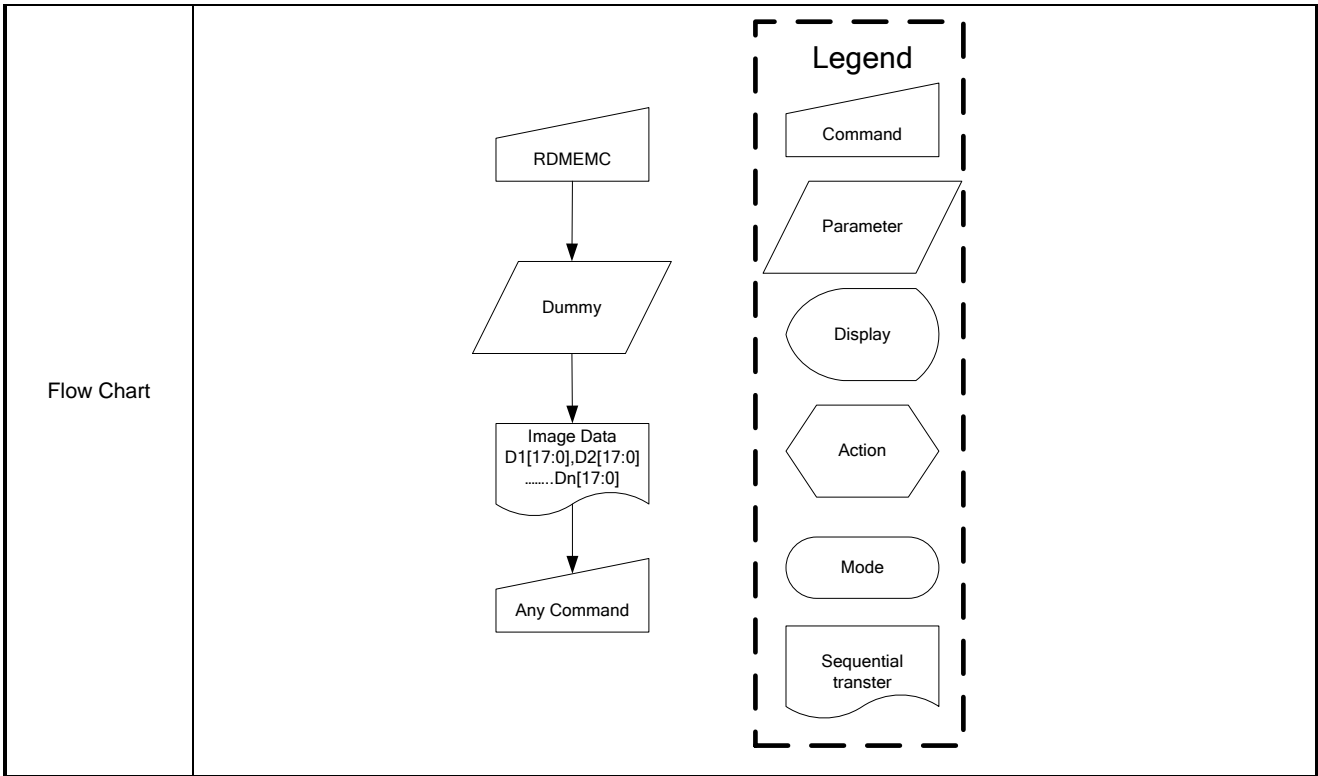
WRMEMC (3Ch): Write Memory Continue

3CH	WRMEMC (Write Memory Continue)												HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
WRMEMC	0	↑	1	-	0	0	1	0	1	1	0	0	(3Ch)
1 ST parameter	1	↑	1	-	D1.7-0							-	
⋮	1	↑	1	-	Dx.7-0							-	
N th parameter	1	↑	1	-	Dn.7-0							-	
Description	<p>-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write memory continue or memory write command.</p> <p>-If MV=0: Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored.</p> <p>If MV=1: Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are written to the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command. If the number of pixels exceeds (XE-XS+1)*(YE-YS+1) the extra pixels are ignored.</p>												

	<table border="1"> <thead> <tr> <th>Condition</th> <th>Column</th> <th>Page</th> </tr> </thead> <tbody> <tr> <td>Command 2C is accepted</td> <td>Return to "Start Column"</td> <td>Return to "Start Page"</td> </tr> <tr> <td>Read/Write RAM action</td> <td>Increment by 1</td> <td>No change</td> </tr> <tr> <td>Column value is large than "End Column"</td> <td>Return to "Start Column"</td> <td>Increment by 1</td> </tr> <tr> <td>Page value is large than "End Page"</td> <td>Return to "Start Column"</td> <td>Return to "Start Page"</td> </tr> </tbody> </table>	Condition	Column	Page	Command 2C is accepted	Return to "Start Column"	Return to "Start Page"	Read/Write RAM action	Increment by 1	No change	Column value is large than "End Column"	Return to "Start Column"	Increment by 1	Page value is large than "End Page"	Return to "Start Column"	Return to "Start Page"
Condition	Column	Page														
Command 2C is accepted	Return to "Start Column"	Return to "Start Page"														
Read/Write RAM action	Increment by 1	No change														
Column value is large than "End Column"	Return to "Start Column"	Increment by 1														
Page value is large than "End Page"	Return to "Start Column"	Return to "Start Page"														
Restriction	A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.															
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes			
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
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Sleep In	Yes															
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared							
Status	Default Value															
Power On Sequence	Contents of memory is set randomly															
S/W Reset	Contents of memory is not cleared															
H/W Reset	Contents of memory is not cleared															
Flow Chart	<pre> graph TD WRMEMC[WRMEMC] --> ImageData[Image Data D1[17:0], D2[17:0]Dn[17:0]] ImageData --> AnyCommand[Any Command] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 															

RDMEMC (3Eh): Read Memory Continue

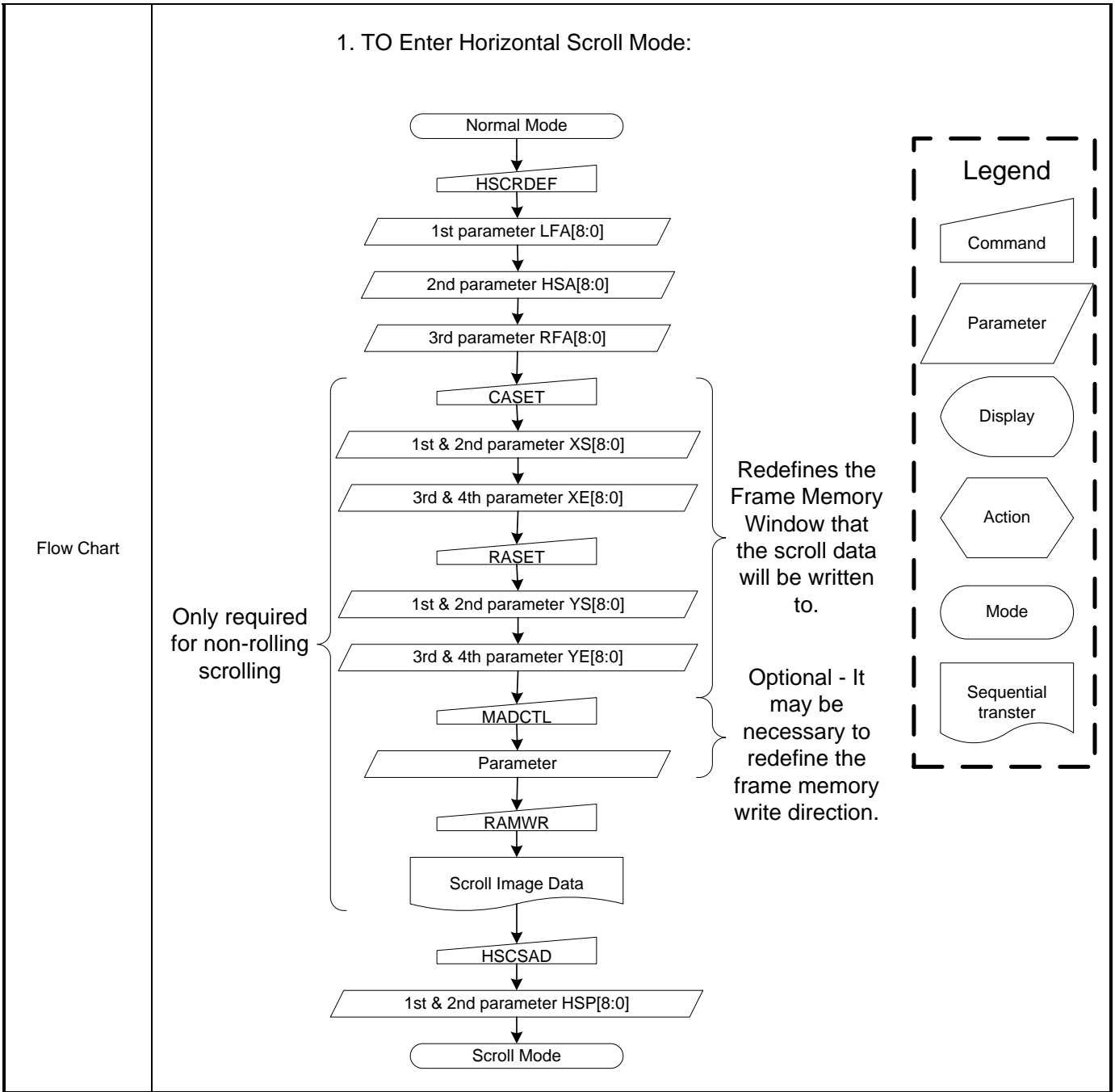
3EH	RDMEMC (Read Memory Continue)																								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RDMEMC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)												
1 ST parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-												
2 nd parameter	1	1	↑	-	D1.7-0							-													
⋮	1	1	↑	-	Dx.7-0							-													
(N+1) th parameter	1	1	↑	-	Dn.7-0							-													
Description	<p>-This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous read memory continue or memory read command.</p> <p>-If MV=0: Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the end column (XE) value. The column register is then reset to XS and the page register is incremented. Pixels are read from the frame memory until the page register equals the end page (YE) value and the column register equals the XE value, or the host processor sends another command.</p> <p>If MV=1: Pixels are read continuing from the pixel location after the read range of the previous memory read or read memory continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the end page (YE) value. The page register is then reset to YS and the column register is incremented. Pixels are read from the frame memory until the column register equals the end column (XE) value and the page register equals the YE value, or the host processor sends another command</p>																								
Restriction	Regardless of the color mode set in interface pixel format, the pixel format returned by read memory continue is always 18-bit so there is no restriction on the length of data																								
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>S/W Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>H/W Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared				
Status	Default Value																								
Power On Sequence	Contents of memory is set randomly																								
S/W Reset	Contents of memory is not cleared																								
H/W Reset	Contents of memory is not cleared																								



HSCRDEF (43h): Horizontal Scrolling Definition

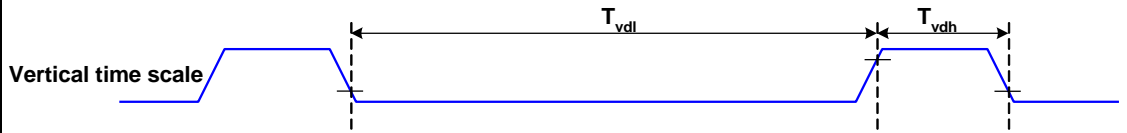
43H	HSCRDEF (Horizontal Scrolling Definition)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
HSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(43h)
1 st parameter	1	↑	1	-	-	-	-	-	-	-	-	LFA.8	(00h)
2 nd parameter	1	↑	1	-	LFA.7-0							(00h)	
3 rd parameter	1	↑	1	-	-	-	-	-	-	-	-	HSA.8	(01h)
4 th parameter	1	↑	1	-	HSA.7-0							(68h)	
5 th parameter	1	↑	1	-	-	-	-	-	-	-	-	RFA.8	(00h)
6 th parameter	1	↑	1	-	RFA.7-0							(00h)	
Description	<p>-This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll</p> <p>-When MADCTL HSD=0</p> <p>-The 1st & 2nd parameter LFA [8:0] describes the Left Fixed Area (in No. of columns from Left of the Frame Memory and Display).</p> <p>-The 3rd & 4th parameter HSA [8:0] describes the width of the Horizontal Scrolling Area (in No. of columns of the Frame Memory [not the display] from the Horizontal Scrolling Start Address) The first columns appears immediately after the right most columns of the Left Fixed Area.</p> <p>-The 5th & 6th parameter RFA [8:0] describes the Right Fixed Area (in No. of columns from Right of the Frame Memory and Display).</p> <p>- If DUAL_EN set 0, the LFA [8:0] · HSA [8:0] and RFA [8:0] only can be set to times of 12. (0, 12, 24, 36,....., 324, 336, 348, 360)</p> <p>- If DUAL_EN set 1, the LFA [8:0] · HSA [8:0] and RFA [8:0] only can be set to times of 24. (0, 24, 48, 72,....., 288, 312, 336, 360)</p> <p>LFA, HSA and RFA refer to the Frame Memory columns Pointer</p> <div style="text-align: center;"> </div>												
Restriction	<p>The condition is $LFA+HSA+RFA = 360$, otherwise Scrolling mode is undefined.</p> <p>In Horizontal Scrolling Mode, MADCTL parameter MV should be set to '0' – this only affects the Frame Memory write.</p>												

Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td>Sleep In</td> <td colspan="2">Yes</td> </tr> </tbody> </table>			Status	Availability		Normal Mode On, Idle Mode Off, Sleep Out	Yes		Normal Mode On, Idle Mode On, Sleep Out	Yes		Partial Mode On, Idle Mode Off, Sleep Out	Yes		Partial Mode On, Idle Mode On, Sleep Out	Yes		Sleep In	Yes	
	Status	Availability																			
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Sleep In	Yes																				
Default	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="3">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>LFA[8:0] = 0000h</td> <td>HSA[8:0] = 0168h</td> <td>RFA[8:0] = 0000h</td> </tr> <tr> <td>S/W Reset</td> <td>LFA[8:0] = 0000h</td> <td>HSA[8:0] = 0168h</td> <td>RFA[8:0] = 0000h</td> </tr> <tr> <td>H/W Reset</td> <td>LFA[8:0] = 0000h</td> <td>HSA[8:0] = 0168h</td> <td>RFA[8:0] = 0000h</td> </tr> </tbody> </table>			Status	Default Value			Power On Sequence	LFA[8:0] = 0000h	HSA[8:0] = 0168h	RFA[8:0] = 0000h	S/W Reset	LFA[8:0] = 0000h	HSA[8:0] = 0168h	RFA[8:0] = 0000h	H/W Reset	LFA[8:0] = 0000h	HSA[8:0] = 0168h	RFA[8:0] = 0000h		
	Status	Default Value																			
	Power On Sequence	LFA[8:0] = 0000h	HSA[8:0] = 0168h	RFA[8:0] = 0000h																	
	S/W Reset	LFA[8:0] = 0000h	HSA[8:0] = 0168h	RFA[8:0] = 0000h																	
H/W Reset	LFA[8:0] = 0000h	HSA[8:0] = 0168h	RFA[8:0] = 0000h																		



TESLWR (44h): Write Tear Scanline

44H	STE (Write Tear Scanline)												HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TESLWR	0	↑	1	-	0	1	0	0	0	1	0	0	(44h)
1 st parameter	1	↑	1	-	-	-	-	-	N.11-8				(00h)
2 nd parameter	1	↑	1	-	N.7-0							(00h)	
Description	<p>-This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MV.</p> <p>-The tearing effect line on has one parameter that describes the tearing effect output line mode.</p> <p>-The tearing effect output line consist of V-blanking information only.</p>												



Note that set tear scanline with N=0 is equivalent to tearing effect line on with TEM=0.

The tearing effect output line shall be active low when the display module is in sleep mode

Restriction

This command takes effect on the frame following the current frame. Therefore, if the tear effect (TE) output is already on, the TE output shall continue to operate as programmed by the previous tearing effect line on or set tear scanline command until the end of the frame

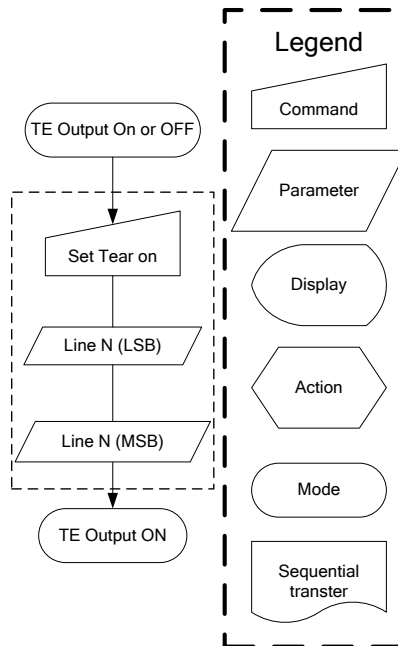
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

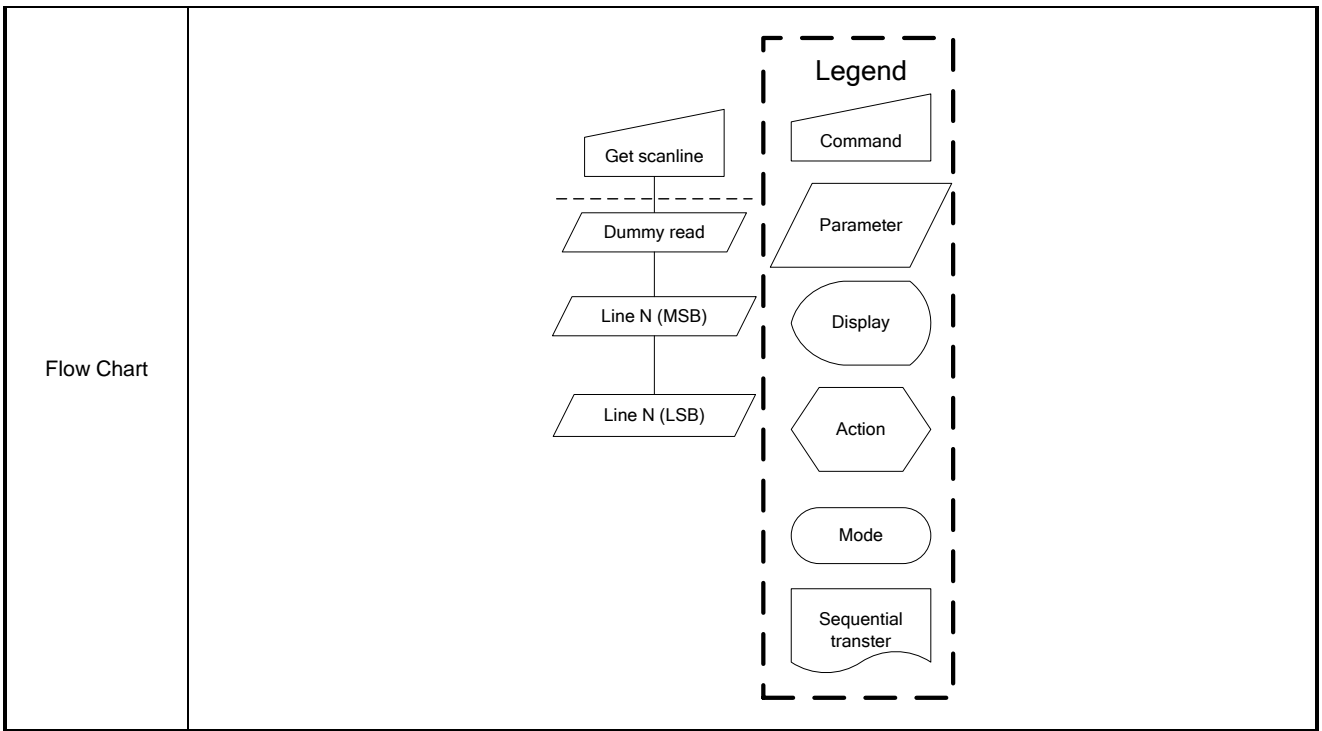
Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



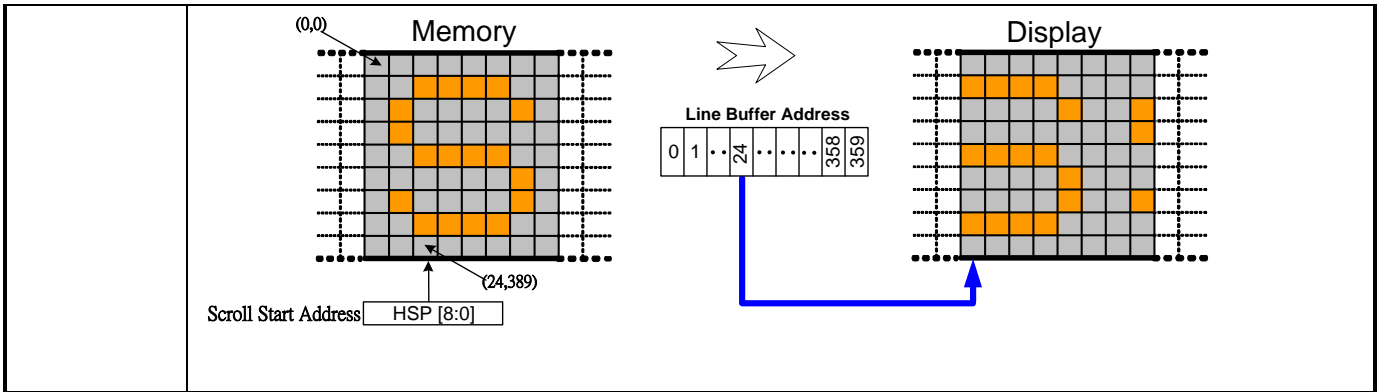
TESLRD (45h): Read Tear Scanline

45H	TESLRD (Read Tear Scanline)																								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
TESLRD	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)												
1 st parameter	1	1	↑	-	-	-	-	-	N.11-8			(00h)													
2 nd parameter	1	1	↑	-	N.7-0							(00h)													
Description	<p>-The display module returns the current scanline ,N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.</p> <p>-When in sleep in mode, the value returned by get scanline is undefined.</p> <p>Note: that Set Tear Scan Line with N = 0 is equivalent to Tearing Effect Line ON with M = 0.</p>																								
Restriction	-																								
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																								
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Status	Default Value																								
Power On Sequence	0000h																								
S/W Reset	0000h																								
H/W Reset	0000h																								



HSCSAD (47h): Horizontal Scroll Start Address of RAM

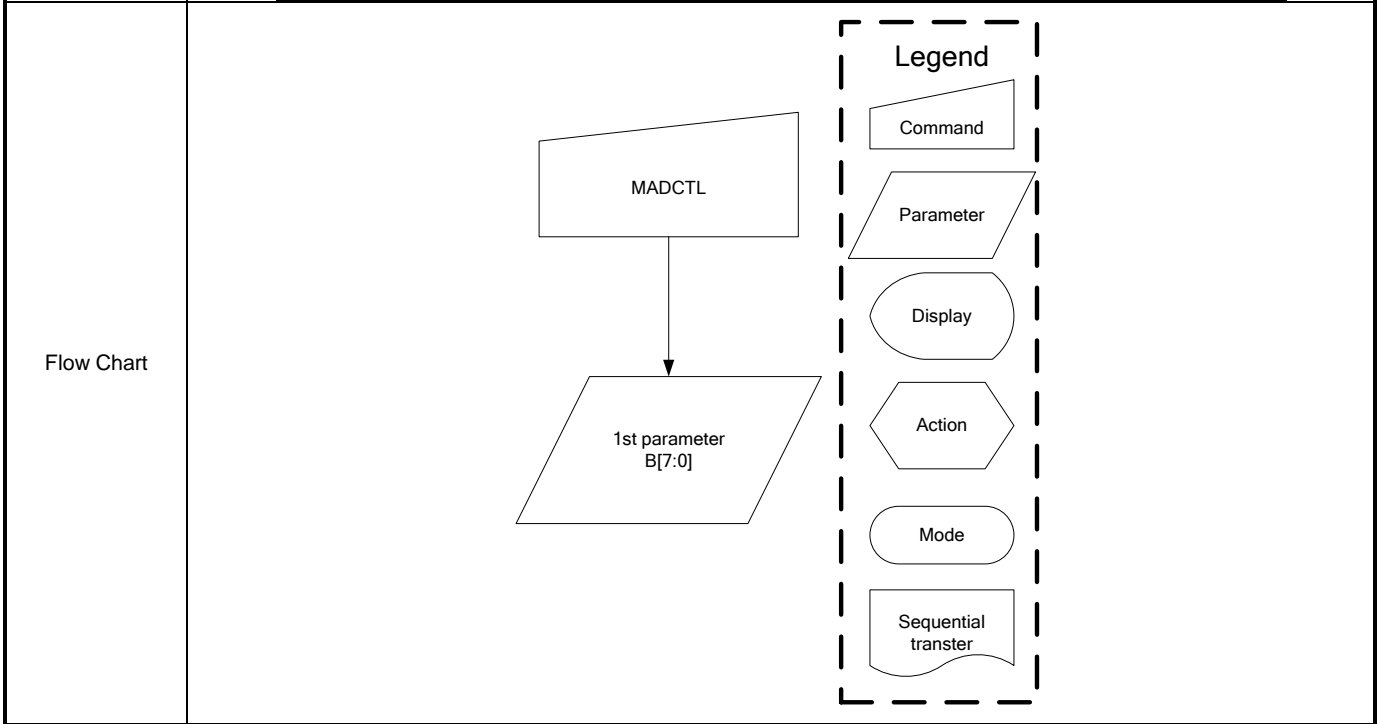
47H	HSCSAD (Horizontal Scroll Start Address of RAM)												HEX
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
HSCSAD	0	↑	1	-	0	1	0	0	0	1	1	1	(47h)
1 ST parameter	1	↑	1	-	0	0	0	0	0	0	0	HSP.8	(00h)
2 ND parameter	1	↑	1	-	HSP.7-0							(00h)	
Description	<p>- If DUAL_EN set 0, the HSP[8:0] only can be set to times of 12. (0, 12, 24, 36, ..., 324, 336, 348, 360)</p> <p>- If DUAL_EN set 1, the HSP[8:0] only can be set to times of 24. (0, 24, 48, 72, ..., 288, 312, 336, 360)</p> <p>When HSD=0</p> <p>Example:</p> <p>When HSP[7:0] = 24</p> <p>When HSD=1</p> <p>Example:</p> <p>When HSP[7:0] = 24</p>												



Register availability Since the value of the horizontal scrolling start address is absolute (with reference to the frame memory), it must not enter the fixed area (defined by Horizontal Scrolling Definition (43h)- otherwise undesirable image will be displayed on the panel)

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	No change
H/W Reset	0000h



RAMCLACT (4Ch): Memory Clear Act

4CH	RAMCLACT (Memory Clear Act)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMCLACT	0	↑	1	-	0	1	0	0	1	1	0	0	(4Ch)
parameter	1	↑	1	-	-	-	-	-	-	-	-	FILLEN	(00h)
Description	FILLEN:												

	<p>"0": No Function.</p> <p>"1": Trigger IC to fill all pixels data in RAM.</p>												
Restriction													
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Status	Default Value												
Power On Sequence	0000-0000												
S/W Reset	0000-0000												
H/W Reset	0000-0000												
Flow Chart													

RAMCLSETR (4Dh): Memory Clear Set R

4DH	RAMCLSETR (Memory Clear Set R)																								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RAMCLSETR	0	↑	1	-	0	1	0	0	1	1	0	1	(4Dh)												
parameter	1	↑	1	-	R.5-0						-	-	(00h)												
Description	R[5:0]: Red subpixel data setting																								
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	0000-0000																								
S/W Reset	0000-0000																								
H/W Reset	0000-0000																								

Flow Chart	
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RAMCLSETG (4Eh): Memory Clear Set G

4EH	RAMCLSETG (Memory Clear Set G)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMCLSETG	0	↑	1	-	0	1	0	0	1	1	1	0	(4Eh)
parameter	1	↑	1	-	G.5-0						-	-	(00h)
Description	G[5:0]: Green subpixel data setting												
Register availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In						Yes						
Default	Status						Default Value						
	Power On Sequence						0000-0000						
	S/W Reset						0000-0000						
	H/W Reset						0000-0000						
Flow Chart													

RAMCLSETB (4Fh): Memory Clear Set B

4FH	RAMCLSETB (Memory Clear Set B)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RAMCLSETB	0	↑	1	-	0	1	0	0	1	1	1	1	(4Fh)
parameter	1	↑	1	-	B.5-0						-	-	(00h)
Description	B[5:0]: Blue subpixel data setting												
Register availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In						Yes						

Default	Status		Default Value	
	Power On Sequence		0000-0000	
	S/W Reset		0000-0000	
	H/W Reset		0000-0000	
Flow Chart				

CDCCTR (50h): CDC Control

50H	CDCCTR (CDC Control)																								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
CDCCTR	0	↑	1	-	0	1	0	1	0	0	0	0	(50h)												
1 st parameter	1	↑	1	-	CDC_EN	CDC_CO MP_EN	CDC_CO MP_MODE	CDC_SI DE_EN	CDC_NO TCH1_EN	CDC_NO TCH2_EN	-	-	(50h)												
Description																									
Restriction																									
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence																									
S/W Reset																									
H/W Reset																									
Flow Chart																									

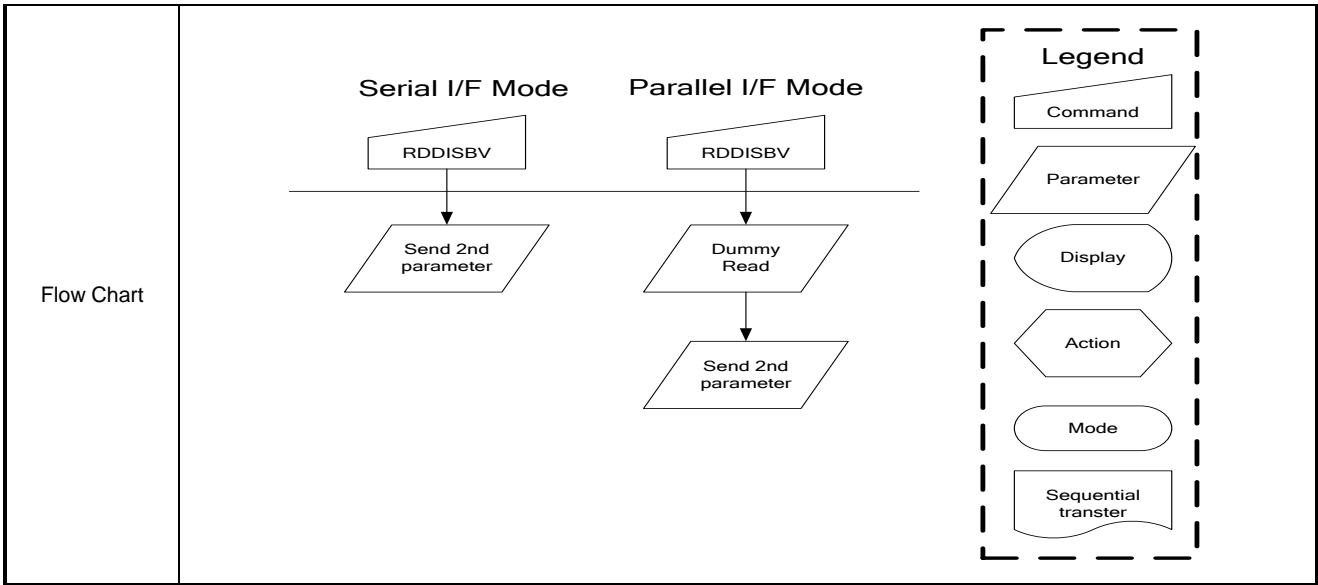
WRDISBV (51h): Write Display Brightness

51H	WRDISBV (Write Display Brightness)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)
Parameter	1	↑	1	-	DBV.7-0							(00h)	
Description	-This command is used to adjust the brightness value of the display.												

	<p>-It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification.</p> <p>-In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p>												
Restriction													
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Power On Sequence	0000h												
S/W Reset	0000h												
H/W Reset	0000h												
Flow Chart	<pre> graph TD A[WRDISBV] --> B[DBV[7:0]] B --> C[New Display Luminance Value Loaded] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

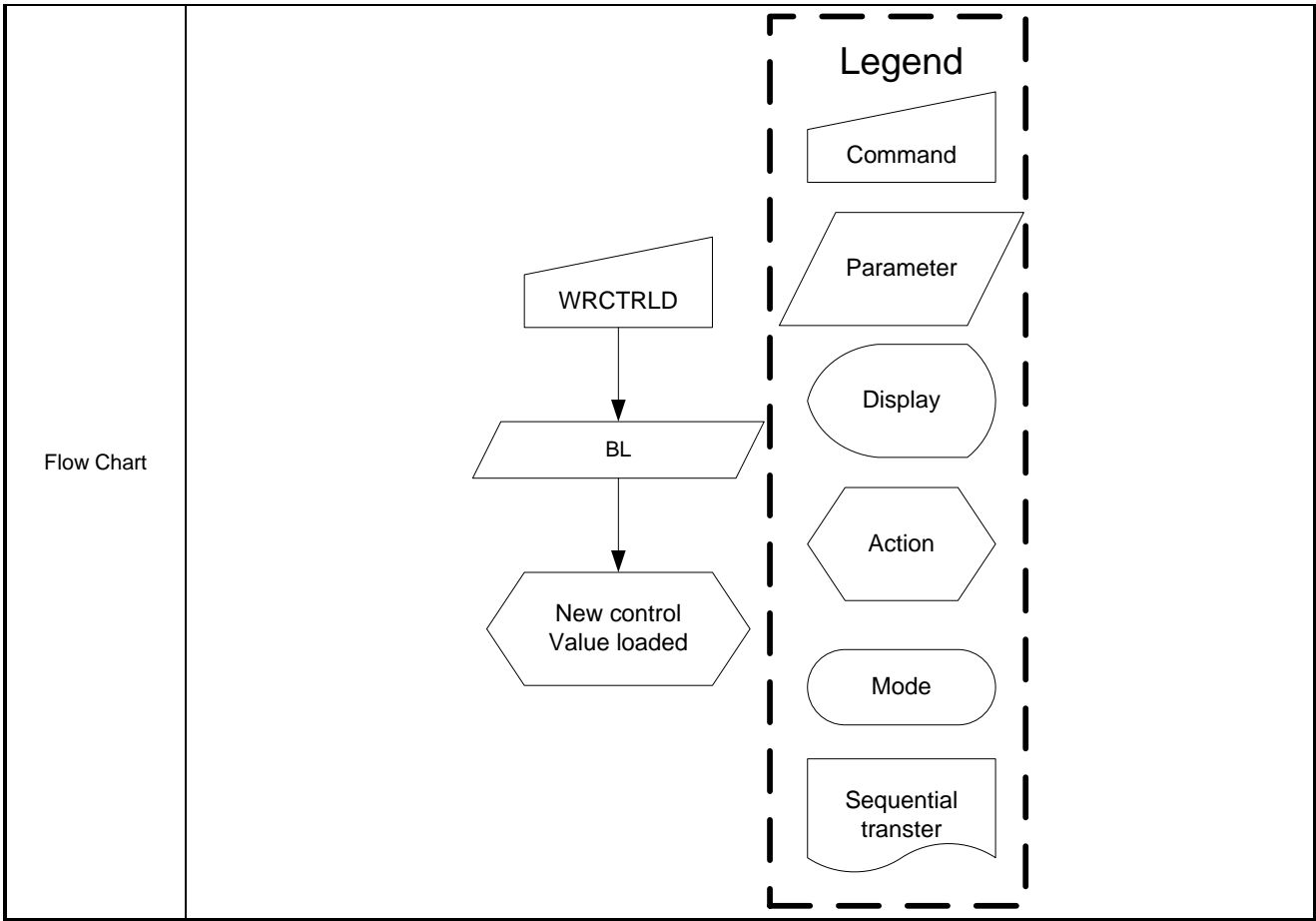
RDDISBV (52h): Read Display Brightness

52H	RDDISBV (Read Display Brightness Value)																								
Inst / Para	D/CX	WRX	RDY	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)												
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-													
2 nd parameter	1	1	↑	-	DBV.7-0							(00h)													
Description	<p>-This command returns the brightness value of the display.</p> <p>-It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is.</p> <p>-In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>-DBV[7:0] is reset when display is in sleep in mode.</p> <p>-DBV[7:0] is '0' when bit BCTRL of write CTRL display command (53h) is '0'</p> <p>-DBV[7:0] IS manual set brightness specified with write CTRL display command (53h) when bit BCTRL is '1'</p>																								
Restriction	-																								
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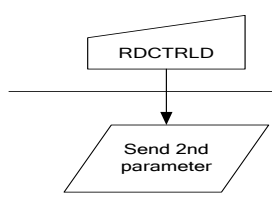
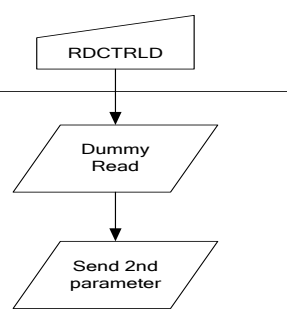
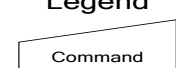



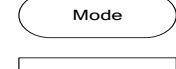
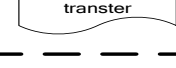
WRCTRLD (53h): Write CTRL Display

53H	WRCTRLD (Write CTRL Display)																								
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)												
Parameter	1	↑	1	-	-	-	-	-	-	BL	-	-	(00h)												
Description	-This command is used to control display brightness. -BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On																								
Restriction																									
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	0000h																								
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RDCTRLD (54h): Read CTRL Display

54H	RDCTRLD (Read CTRL value Display)												HEX										
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)										
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-											
2 nd parameter	1	1	↑	-	-	-	-	-	-	BL	-	-	(00h)										
Description	-This command returns ambient light and brightness control values. -BL: Backlight Control On/Off 0 = Off 1 = On																						
Restriction	-																						
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	Power On Sequence	0000h									
	S/W Reset	0000h									
H/W Reset	0000h										
<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Serial I/F Mode</p>  </div> <div style="text-align: center;"> <p>Parallel I/F Mode</p>  </div> </div>											
<div style="border: 1px dashed black; padding: 5px;"> <p style="text-align: center;">Legend</p> <ul style="list-style-type: none">  Command  Parameter  Display  Action  Mode  Sequential transfer </div>											
Flow Chart											

CPRAMWR (6Ch): Compress Memory Write

6CH	CPRAMWR (Compress Memory Write)												HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CPRAMWR	0	↑	1	-	0	1	1	0	1	1	0	0	(6Ch)
parameter	1	↑	1	-	Write data stream							(00h)	
Description	<p>-For 262K Color Format: (when GCOMPR_C262 = 1 in command 6Fh)</p> <p>D[7:2]: 6-bit Red subpixel data setting</p> <p>D[15:10]: 6-bit Green subpixel data setting</p> <p>D[23:18]: 6-bit Blue subpixel data setting</p> <p>D[31:24]: Pixel number N = D[31:24] + 1. (N = 1~256)</p> <p>Trigger IC to fill N pixels (the pixel data is depend on D[23:2] setting) to RAM when D[31:24] is set.</p> <p>-For 65K Color Format: (when GCOMPR_C262 = 0 in command 6Fh)</p> <p>D[7:3]: 5-bit Red subpixel data setting</p> <p>D[2:0] + MCW[15:13]: 6-bit Green subpixel data setting</p> <p>D[12:8]: 5-bit Blue subpixel data setting</p> <p>D[23:16]: Pixel number N = D[23:16] + 1. (N=1~256)</p> <p>Trigger IC to fill N pixels (the pixel data is depend on D[15:0] setting) to RAM when D[23:16] is set.</p>												

	D[31:24]: No function.												
Restriction													
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Power On Sequence	Contents of memory is set randomly												
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Flow Chart													

CPRAMWRC (6Dh): Compress Continue Write

6DH	CPRAMWRC (Compress Continue Write)												HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CPRAMWRC	0	↑	1	-	0	1	1	0	1	1	0	1	(6Dh)
parameter	1	↑	1	-	Write data stream							(00h)	
Description	<p>-For 262K Color Format: (when GCOMPR_C262 = 1 in command 6Fh)</p> <p>D[7:2]: 6-bit Red subpixel data setting</p> <p>D[15:10]: 6-bit Green subpixel data setting</p> <p>D[23:18]: 6-bit Blue subpixel data setting</p> <p>D[31:24]: Pixel number N = D[31:24] + 1. (N = 1~256)</p> <p>Trigger IC to fill N pixels (the pixel data is depend on D[23:2] setting) to RAM when D[31:24] is set.</p> <p>-For 65K Color Format: (when GCOMPR_C262 = 0 in command 6Fh)</p> <p>D[7:3]: 5-bit Red subpixel data setting</p> <p>D[2:0] + MCW[15:13]: 6-bit Green subpixel data setting</p> <p>D[12:8]: 5-bit Blue subpixel data setting</p> <p>D[23:16]: Pixel number N = D[23:16] + 1. (N=1~256)</p> <p>Trigger IC to fill N pixels (the pixel data is depend on D[15:0] setting) to RAM when D[23:16] is set.</p> <p>D[31:24]: No function.</p>												
Restriction													

Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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	Status	Default Value												
	Power On Sequence	Contents of memory is set randomly												
	S/W Reset	Contents of memory is not cleared												
H/W Reset	Contents of memory is not cleared													
Flow Chart														

CPCTRL (6Fh): Compress CTRL

6FH	CPCTRL (Compress CTRL)													
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
CPCTRL	0	↑	1	-	0	1	1	0	1	1	1	1	(6Fh)	
parameter	1	↑	1	-	GCOMPR_C262	-	-	GCOMPR_EN	-	-	-	RDY	(00h)	
Description	<p>GCOMPR_EN: "0": disable Memory Compression Write function. "1": enable Memory Compression Write function.</p> <p>GCOMPR_C262 : "0": 65K color for command 6Ch and 6Dh "1": 262K color for command 6Ch and 6Dh</p>													
Restriction														
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													

Default	Status		Default Value	
	Power On Sequence			
	S/W Reset			
	H/W Reset			
Flow Chart				

RDID1 (DAh): Read ID1

DAH	RDID1 (Read ID1)												HEX												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)												
parameter	1	1	↑	-	-	ID1.6-0						(7Fh)													
Description	-This read byte identifies the LCD module's manufacturer. ↑: Don't care.																								
Register availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	7Fh																								
S/W Reset	7Fh																								
H/W Reset	7Fh																								

RDID2 (DBh): Read ID2

DBH	RDID2 (Read ID2)												HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)
1 st parameter	1	1	↑	-	-	ID2.6-0						(7Fh)	
Description	This read byte is used to track the LCD module/driver IC version. ↑: Don't care.												
Register availability													

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Status	Default Value													
Power On Sequence	7Fh													
S/W Reset	7Fh													
H/W Reset	7Fh													

RDID3 (DCh): Read ID3

DCH	RDID3 (Read ID3)												HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)
1 st parameter	1	1	↑	-	-	ID3.6-0						(7Fh)	
Description	This read byte identifies the LCD module/driver. '↑': Don't care.												
Register availability													
Default													

13.3 Command Table 2

COMMAND Table 2														
Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
OTP MODE SEL	0	↑	1	-	1	0	1	0	0	0	0	0	(A0h)	OTP MODE SEL
	1	↑	1		OTP_DUM P	BIT_PRO G	PTM.1-0		EXT_VPP	INT_VPP	OTP_EN	RDY		
OTP PAGE ADDR	0	↑	1	-	1	0	1	0	0	0	1	1	(A3h)	OTP PAGE ADDR
	1	↑	1		PA.7-0									
OTP DATA IN (DUMP RD)	0	↑	1	-	1	0	1	0	0	1	0	0	(A4h)	OTP DATA IN (DUMP RD)
	1	↑	1		PDIN.7-0									
OTP CMD ACK	0	↑	1	-	1	0	1	0	0	1	0	1	(A5h)	OTP CMD ACK
	1	↑	1		-	-	-	-	-	-	-	-	-	
GVDD SET	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)	GVDD SET
	1	↑	1		-	VRHP.6-0								
GVCL SET	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	GVCL SET
	1	↑	1		VRHN.6-0									
VCOM GND SET	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	VCOM GND SET
	1	↑	1		VCM.6-0									
GVDD_GVEE_S ET	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)	GVDD_GVEE E_SET
	1	↑	1		GVEE_AD.3-0				GVDD_AD.3-0					
STEP SET1	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)	STEP SET1
	1	↑	1		-	AVCLS.2-0			-	AVDDS.2-0				

COMMAND Table 2

Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
STEP SET2	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)	STEP SET2
	1	↑	1		VGLS.3-0				VGHS.3-0					
SVDD_SVCL_SE T	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)	SVDD_SVCL _SET
	1	↑	1		-	SELN.2-0			-	-	SELP.1-0			
TCON_SET	0	↑	1	-	1	0	1	1	1	0	1	0	(BAh)	TCON_SET
	1	↑	1		-	GATE_TUNE.2-0				-	-	NLINE.1-0		
RGB_VBP	0	↑	1	-	1	0	1	1	1	0	1	1	(BBh)	RGB_VBP
	1	↑	1		-	VBP.6-0								
RGB_HBP	0	↑	1	-	1	0	1	1	1	1	0	0	(BCh)	RGB_HBP
	1	↑	1		-	HBP.6-0								
RGB_SET	0	↑	1	-	1	0	1	1	1	1	0	1	(BDh)	RGB_SET
	1	↑	1		WO	-	-	RCM	RGB_VDP OL_XOR	RGB_HDP OL_XOR	RGB_DEP OL_XOR	RGB_DCL KPOL_XO R		
CABC_SET1	0	↑	1	-	1	0	1	1	1	1	1	0	(BEh)	CABC_SET1
	1	↑	1		-	-	-	LED_PWM _OEX	-	DSPOFFP WM_MD	PWM_FIX ON	PWM_PO LAR		
CABC_SET2	0	↑	1	-	1	0	1	1	1	1	1	1	(BFh)	CABC_SET2
	1	↑	1		-	PWM_SE GMENT[2]	PWM_SE GMENT[1]	PWM_SE GMENT[0]	-	PWM_CLK _SEL[2]	PWM_CLK _SEL[1]	PWM_CLK _SEL[0]		
FRCTRA1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)	FRCTRA1
	1	↑	1		NLA	-	-	BPFPA.12-8						
FRCTRA2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)	FRCTRA2
	1	↑	1		BPFPA.7-0									
FRCTRA3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)	FRCTRA3
	1	↑	1		RTNA.7-0									
FRCTRB1	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)	FRCTRB1
	1	↑	1		NLB	-	-	BPFPA.12-8						
FRCTRB2	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)	FRCTRB2
	1	↑	1		BPFPA.7-0									
FRCTRB3	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)	FRCTRB3
	1	↑	1		RTNB.7-0									
PWRCTRA1	0	↑	1	-	1	1	0	0	0	1	1	0	(C6h)	PWRCTRA1
	1	↑	1		DCA3.1-0		DCA2S.1-0		DCA2.1-0		DCA1.1-0			

COMMAND Table 2

Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PWRCTRA2	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)	PWRCTRA2
	1	↑	1		-	APA.2-0			SAPA.1-0		DCA4.1-0			
PWRCTRA3	0	↑	1	-	1	1	0	0	1	0	0	0	(C8h)	PWRCTRA3
	1	↑	1		CLK_SNA.1-0	CLK_SPA.1-0		-	-	CLK_HYA.1-0				
PWRCTRB1	0	↑	1	-	1	1	0	0	1	0	0	1	(C9h)	PWRCTRB1
	1	↑	1		DCB3.1-0	DCB2S.1-0		DCB2.1-0		DCB1.1-0				
PWRCTRB2	0	↑	1	-	1	1	0	0	1	0	1	0	(CAh)	PWRCTRB2
	1	↑	1		-	APB.2-0			SAPB.1-0		DCB4.1-0			
PWRCTRB3	0	↑	1	-	1	1	0	0	1	0	1	1	(CBh)	PWRCTRB3
	1	↑	1		CLK_SNB.1-0	CLK_SPB.1-0		-	-	CLK_HYB.1-0				
DSTB_DSLP	0	↑	1	-	1	1	0	0	1	1	1	1	(CFh)	DSTB_DSLP
	1	↑	1		-	-	-	-	-	DSTB_EN	DSLTP_EN			
RES_SET1	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)	RES_SET1
	1	↑	1		DUAL_EN	SSI	-	X_RES.8	-	Y_RES.10-8				
RES_SET2	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)	RES_SET2
	1	↑	1		X_RES.7-0									
RES_SET3	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	RES_SET3
	1	↑	1		Y_RES.7-0									
Flicker_ADJ	0	↑	1	-	1	1	0	1	1	1	0	1	(DDh)	Flicker_ADJ
	1	↑	1		-	VMF.6-0								
Flicker_ADJ_NE W	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)	Flicker_ADJ_ NEW
	1	↑	1		-	VMF_NEW.6-0								
GAMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E0)	GAMCTRP1
	1	↑	1		VC63P.3-0				VC0P.3-0					
	1	↑	1		-	-	VC1P.5-0							
	1	↑	1		-	-	VC2P.5-0							
	1	↑	1		-	-	-	VC4P.4-0						
	1	↑	1		-	-	-	VC6P.4-0						
	1	↑	1		-	AJ0P.2-0			VC13P.3-0					
	1	↑	1		-	VC20P.6-0								
	1	↑	1		-	VC36P.2-0			-	VC27P.2-0				
	1	↑	1		-	VC43P.6-0								
	1	↑	1		-	AJ1P.2-0			VC50P.3-0					
	1	↑	1		-	-	-	VC57P.4-0						

COMMAND Table 2

Instruction	D/CX	WRX	RDX	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function	
	1	↑	1		-	-	-	VC59P.4-0							
	1	↑	1		-	-		VC61P.5-0							
	1	↑	1		-	-		VC62P.5-0							
GAMCTRN1	0	↑	1		1	1	1	0	0	0	0	1	(E1)		
	1	↑	1		VC63N.3-0				VC0N.3-0						
	1	↑	1		-	-	VC1N.5-0								
	1	↑	1		-	-	VC2N.5-0								
	1	↑	1		-	-	-	VC4N.4-0							
	1	↑	1		-	-	-	VC6N.4-0							
	1	↑	1		-	AJ0N.2-0			VC13N.3-0						
	1	↑	1		-	VC20N.6-0									GAMCTRN1
	1	↑	1		-	VC36N.2-0			-	VC27N.2-0					
	1	↑	1		-	VC43N.6-0									
	1	↑	1		-	AJ1N.2-0			VC50N.3-0						
	1	↑	1		-	-	-	VC57N.4-0							
	1	↑	1		-	-	-	VC59N.4-0							
	1	↑	1		-	-	VC61N.5-0								
	1	↑	1		-	-	VC62N.5-0								

VRHPS (B0h): VRHP Set

B0H	VRHPS (VRHP Set)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VRHP SET	0	↑	1	-	1	0	1	1	0	0	0	0	(B0h)
1 st Parameter	1	↑	1	-	-	VRHP.6-0						(66h)	
Description	VRHP[6:0]: VRHP Set.												
		VRHP[6:0]	VAP(GVDD) (V)				VRHP[6:0]	VAP(GVDD) (V)					
		00h	3.650 + (vcom offset)				40h	5.250 + (vcom offset)					
		01h	3.675 + (vcom offset)				41h	5.275 + (vcom offset)					
		02h	3.700 + (vcom offset)				42h	5.300 + (vcom offset)					
		03h	3.725 + (vcom offset)				43h	5.325 + (vcom offset)					
		04h	3.750 + (vcom offset)				44h	5.350 + (vcom offset)					
	05h	3.775 + (vcom offset)				45h	5.375 + (vcom offset)						

06h	3.800 + (vcom offset)	46h	5.400 + (vcom offset)
07h	3.825 + (vcom offset)	47h	5.425 + (vcom offset)
08h	3.850 + (vcom offset)	48h	5.450 + (vcom offset)
09h	3.875 + (vcom offset)	49h	5.475 + (vcom offset)
0Ah	3.900 + (vcom offset)	4Ah	5.500 + (vcom offset)
0Bh	3.925 + (vcom offset)	4Bh	5.525 + (vcom offset)
0Ch	3.950 + (vcom offset)	4Ch	5.550 + (vcom offset)
0Dh	3.975 + (vcom offset)	4Dh	5.575 + (vcom offset)
0Eh	4.000 + (vcom offset)	4Eh	5.600 + (vcom offset)
0Fh	4.025 + (vcom offset)	4Fh	5.625 + (vcom offset)
10h	4.050 + (vcom offset)	50h	5.650 + (vcom offset)
11h	4.075 + (vcom offset)	51h	5.675 + (vcom offset)
12h	4.100 + (vcom offset)	52h	5.700 + (vcom offset)
13h	4.125 + (vcom offset)	53h	5.725 + (com offset)
14h	4.150 + (vcom offset)	54h	5.750 + (vcom offset)
15h	4.175 + (vcom offset)	55h	5.775 + (vcom offset)
16h	4.200 + (vcom offset)	56h	5.800 + (vcom offset)
17h	4.225 + (vcom offset)	57h	5.825 + (vcom offset)
18h	4.250 + (vcom offset)	58h	5.850 + (vcom offset)
19h	4.275 + (vcom offset)	59h	5.875 + (vcom offset)
1Ah	4.300 + (vcom offset)	5Ah	5.900 + (vcom offset)
1Bh	4.325 + (vcom offset)	5Bh	5.925 + (vcom offset)
1Ch	4.350 + (vcom offset)	5Ch	5.950 + (vcom offset)
1Dh	4.375 + (vcom offset)	5Dh	5.975 + (vcom offset)
1Eh	4.400 + (vcom offset)	5Eh	6.000 + (vcom offset)
1Fh	4.425 + (vcom offset)	5Fh	6.025 + (vcom offset)
20h	4.450 + (vcom offset)	60h	6.050 + (vcom offset)
21h	4.475 + (vcom offset)	61h	6.075 + (vcom offset)
22h	4.500 + (vcom offset)	62h	6.100 + (vcom offset)
23h	4.525 + (vcom offset)	63h	6.125 + (vcom offset)
24h	4.550 + (vcom offset)	64h	6.150 + (vcom offset)
25h	4.575 + (vcom offset)	65h	6.175 + (vcom offset)
26h	4.600 + (vcom offset)	66h	6.200 + (vcom offset)
27h	4.625 + (vcom offset)	67h	6.225 + (vcom offset)
28h	4.650 + (vcom offset)	68h	6.250 + (vcom offset)
29h	4.675 + (vcom offset)	69h	6.275 + (vcom offset)
2Ah	4.700 + (vcom offset)	6Ah	6.300 + (vcom offset)

	2Bh	4.725 + (vcom offset)	6Bh	6.325 + (vcom offset)
	2Ch	4.750 + (vcom offset)	6Ch	6.350 + (vcom offset)
	2Dh	4.775 + (vcom offset)	6Dh	6.375 + (vcom offset)
	2Eh	4.800 + (vcom offset)	6Eh	6.400 + (vcom offset)
	2Fh	4.825 + (vcom offset)	6Fh	6.425 + (vcom offset)
	30h	4.850 + (vcom offset)	70h	6.450 + (vcom offset)
	31h	4.875 + (vcom offset)	71h	6.475 + (vcom offset)
	32h	4.900 + (vcom offset)	72h	6.500 + (vcom offset)
	33h	4.925 + (vcom offset)	73h	6.525 + (vcom offset)
	34h	4.950 + (vcom offset)	74h	6.550 + (vcom offset)
	35h	4.975 + (vcom offset)	75h	6.575 + (vcom offset)
	36h	5.000 + (vcom offset)	76h	6.600 + (vcom offset)
	37h	5.025 + (vcom offset)	77h	6.625 + (vcom offset)
	38h	5.050 + (vcom offset)	78h	6.650 + (vcom offset)
	39h	5.075 + (vcom offset)	79h	6.675 + (vcom offset)
	3Ah	5.100 + (vcom offset)	7Ah	6.700 + (vcom offset)
	3Bh	5.125 + (vcom offset)	7Bh	6.725 + (vcom offset)
	3Ch	5.150 + (vcom offset)	7Ch	6.750 + (vcom offset)
	3Dh	5.175 + (vcom offset)	7Dh	6.775 + (vcom offset)
	3Eh	5.200 + (vcom offset)	7Eh	6.800 + (vcom offset)
	3Fh	5.225 + (vcom offset)	7Fh	6.825 + (vcom offset)
	'-': Don't care			

Register Availability	<table border="1"> <thead> <tr><th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													

Default	<table border="1"> <thead> <tr><th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>66h</td></tr> <tr><td>S/W Reset</td><td>66h</td></tr> <tr><td>H/W Reset</td><td>66h</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	66h	S/W Reset	66h	H/W Reset	66h
	Status	Default Value								
	Power On Sequence	66h								
	S/W Reset	66h								
H/W Reset	66h									

VRHNS (B1h): VRHN Set

B1H	VRHNS (VRHN Set)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VRHN SET	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1 st Parameter	1	↑	1	-	-	VRHN.6-0						(4Dh)	
Description	VRHN[6:0]: VRHN Set.												
	VRHN[6:0]	VAN(GVCL) (V)				VRHN[6:0]	VAP(GVCL) (V)						
	00h	-1.875 + (vcom offset)				40h	-3.475 + (vcom offset)						
	01h	-1.900 + (vcom offset)				41h	-3.500 + (vcom offset)						
	02h	-1.925 + (vcom offset)				42h	-3.525 + (vcom offset)						
	03h	-1.950 + (vcom offset)				43h	-3.550 + (vcom offset)						
	04h	-1.975 + (vcom offset)				44h	-3.575 + (vcom offset)						
	05h	-2.000 + (vcom offset)				45h	-3.600 + (vcom offset)						
	06h	-2.025 + (vcom offset)				46h	-3.625 + (vcom offset)						
	07h	-2.050 + (vcom offset)				47h	-3.650 + (vcom offset)						
	08h	-2.075 + (vcom offset)				48h	-3.675 + (vcom offset)						
	09h	-2.100 + (vcom offset)				49h	-3.700 + (vcom offset)						
	0Ah	-2.125 + (vcom offset)				4Ah	-3.725 + (vcom offset)						
	0Bh	-2.150 + (vcom offset)				4Bh	-3.750 + (vcom offset)						
	0Ch	-2.175 + (vcom offset)				4Ch	-3.775 + (vcom offset)						
	0Dh	-2.200 + (vcom offset)				4Dh	-3.800 + (vcom offset)						
	0Eh	-2.225 + (vcom offset)				4Eh	-3.825 + (vcom offset)						
	0Fh	-2.250 + (vcom offset)				4Fh	-3.850 + (vcom offset)						
	10h	-2.275 + (vcom offset)				50h	-3.875 + (vcom offset)						
	11h	-2.300 + (vcom offset)				51h	-3.900 + (vcom offset)						
	12h	-2.325 + (vcom offset)				52h	-3.925 + (vcom offset)						
	13h	-2.350 + (vcom offset)				53h	-3.950 + (vcom offset)						
	14h	-2.375 + (vcom offset)				54h	-3.975 + (vcom offset)						
	15h	-2.400 + (vcom offset)				55h	-4.000 + (vcom offset)						
	16h	-2.425 + (vcom offset)				56h	-4.025 + (vcom offset)						
	17h	-2.450 + (vcom offset)				57h	-4.050 + (vcom offset)						
	18h	-2.475 + (vcom offset)				58h	-4.075 + (vcom offset)						
	19h	-2.500 + (vcom offset)				59h	-4.100 + (vcom offset)						
1Ah	-2.525 + (vcom offset)				5Ah	-4.125 + (vcom offset)							
1Bh	-2.550 + (vcom offset)				5Bh	-4.150 + (vcom offset)							
1Ch	-2.575 + (vcom offset)				5Ch	-4.175 + (vcom offset)							
1Dh	-2.600 + (vcom offset)				5Dh	-4.200 + (vcom offset)							

1Eh	-2.625 + (vcom offset)	5Eh	-4.225 + (vcom offset)
1Fh	-2.650 + (vcom offset)	5Fh	-4.250 + (vcom offset)
20h	-2.675 + (vcom offset)	60h	-4.275 + (vcom offset)
21h	-2.700 + (vcom offset)	61h	-4.300 + (vcom offset)
22h	-2.725 + (vcom offset)	62h	-4.325 + (vcom offset)
23h	-2.750 + (vcom offset)	63h	-4.350 + (vcom offset)
24h	-2.775 + (vcom offset)	64h	-4.375 + (vcom offset)
25h	-2.800 + (vcom offset)	65h	-4.400 + (vcom offset)
26h	-2.825 + (vcom offset)	66h	-4.425 + (vcom offset)
27h	-2.850 + (vcom offset)	67h	-4.450 + (vcom offset)
28h	-2.875 + (vcom offset)	68h	-4.475 + (vcom offset)
29h	-2.900 + (vcom offset)	69h	-4.500 + (vcom offset)
2Ah	-2.925 + (vcom offset)	6Ah	-4.525 + (vcom offset)
2Bh	-2.950 + (vcom offset)	6Bh	-4.550 + (vcom offset)
2Ch	-2.975 + (vcom offset)	6Ch	-4.575 + (vcom offset)
2Dh	-3.000 + (vcom offset)	6Dh	-4.600 + (vcom offset)
2Eh	-3.025 + (vcom offset)	6Eh	-4.625 + (vcom offset)
2Fh	-3.050 + (vcom offset)	6Fh	-4.650 + (vcom offset)
30h	-3.075 + (vcom offset)	70h	-4.675 + (vcom offset)
31h	-3.100 + (vcom offset)	71h	-4.700 + (vcom offset)
32h	-3.125 + (vcom offset)	72h	-4.725 + (vcom offset)
33h	-3.150 + (vcom offset)	73h	-4.750 + (vcom offset)
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37h	-3.250 + (vcom offset)	77h	-4.850 + (vcom offset)
38h	-3.275 + (vcom offset)	78h	-4.875 + (vcom offset)
39h	-3.300 + (vcom offset)	79h~7Fh	-4.900 + (vcom offset)
3Ah	-3.325 + (vcom offset)	-	-
3Bh	-3.350 + (vcom offset)	-	-
3Ch	-3.375 + (vcom offset)	-	-
3Dh	-3.400 + (vcom offset)	-	-
3Eh	-3.425 + (vcom offset)	-	-
3Fh	-3.450 + (vcom offset)	-	-
'-': Don't care			
Register Availability			

	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>4Dh</td> </tr> <tr> <td>S/W Reset</td> <td>4Dh</td> </tr> <tr> <td>H/W Reset</td> <td>4Dh</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	4Dh	S/W Reset	4Dh	H/W Reset	4Dh				
Status	Default Value												
Power On Sequence	4Dh												
S/W Reset	4Dh												
H/W Reset	4Dh												

VCOMS (B2h): VCOM GND SET

B2H	VCOMS (VCOM GND SET)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCOM GND SET	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1 st Parameter	1	↑	1	-	-	VCM.6-0							(2Ch)
Description	VCM[6:0]: VCM Set.												
	VCM[6:0]	VSF (V)					VCM[6:0]	VSF (V)					
	00h	0.100					40h	1.700					
	01h	0.125					41h	1.725					
	02h	0.150					42h	1.750					
	03h	0.175					43h	1.775					
	04h	0.200					44h	1.800					
	05h	0.225					45h	1.825					
	06h	0.250					46h	1.850					
	07h	0.275					47h	1.875					
	08h	0.300					48h	1.900					
	09h	0.325					49h	1.925					
	0Ah	0.350					4Ah	1.950					
	0Bh	0.375					4Bh	1.975					
	0Ch	0.400					4Ch	2.000					
	0Dh	0.425					4Dh	2.025					
	0Eh	0.450					4Eh	2.050					
0Fh	0.475					4Fh	2.075						

10h	0.500	50h	2.100
11h	0.525	51h	2.125
12h	0.550	52h	2.150
13h	0.575	53h	2.175
14h	0.600	54h	2.200
15h	0.625	55h~7Fh	-
16h	0.650	-	-
17h	0.675	-	-
18h	0.700	-	-
19h	0.725	-	-
1Ah	0.750	-	-
1Bh	0.775	-	-
1Ch	0.800	-	-
1Dh	0.825	-	-
1Eh	0.850	-	-
1Fh	0.875	-	-
20h	0.900	-	-
21h	0.925	-	-
22h	0.950	-	-
23h	0.975	-	-
24h	1.000	-	-
25h	1.025	-	-
26h	1.050	-	-
27h	1.075	-	-
28h	1.100	-	-
29h	1.125	-	-
2Ah	1.150	-	-
2Bh	1.175	-	-
2Ch	1.200	-	-
2Dh	1.225	-	-
2Eh	1.250	-	-
2Fh	1.275	-	-
30h	1.300	-	-
31h	1.325	-	-
32h	1.350	-	-
33h	1.375	-	-
34h	1.400	-	-

35h	1.425	-	-
36h	1.450	-	-
37h	1.475	-	-
38h	1.500	-	-
39h	1.525	-	-
3Ah	1.550	-	-
3Bh	1.575	-	-
3Ch	1.600	-	-
3Dh	1.625	-	-
3Eh	1.650	-	-
3Fh	1.675	-	-

Note:

1. VCOMS is used for feed through voltage compensation.
2. Setting limitation: VCOMS = 0.1V~2.2V.

'-': Don't care

Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes													

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	Status	Default Value								
	Power On Sequence	2Ch								
	S/W Reset	2Ch								
H/W Reset	2Ch									

GAMOPPS (B4h): GVDD_GVEE_SET

B4H	GAMOPPS (GVDD_GVEE_SET)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GVDD_GVEE_SET	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
1 st Parameter	1	↑	1	-	GVEE_AD.3-0			GVDD_AD.3-0			(88h)		
Description	GVEE_AD[3:0]: Negative Gamma OP Power Set.												
	GVEE_AD [3:0]		VNDAC (V)			GVEE_AD [3:0]		VNDAC (V)					
00h		-3.4			08h		-4.2						

	01h	-3.5	09h	-4.3	
	02h	-3.6	0Ah	-4.4	
	03h	-3.7	0Bh	-4.5	
	04h	-3.8	0Ch	-4.6	
	05h	-3.9	0Dh	-4.7	
	06h	-4.0	0Eh	-4.8	
	07h	-4.1	0Fh	-4.9	
	GVDD_AD[3:0]: Positive Gamma OP Power Set.				
	GVDD_AD [3:0]	VPDAC (V)	GVDD_AD [3:0]	VPDAC (V)	
	00h	5.5	08h	6.3	
	01h	5.6	09h	6.4	
	02h	5.7	0Ah	6.5	
	03h	5.8	0Bh	6.6	
	04h	5.9	0Ch	6.7	
	05h	6.0	0Dh	6.8	
06h	6.1	0Eh	6.9		
07h	6.2	0Fh	7.0		
'-': Don't care					
Register Availability	Status		Availability		
	Normal Mode On, Idle Mode Off, Sleep Out		Yes		
	Normal Mode On, Idle Mode On, Sleep Out		Yes		
	Partial Mode On, Idle Mode Off, Sleep Out		Yes		
	Partial Mode On, Idle Mode On, Sleep Out		Yes		
	Sleep In		Yes		
Default	Status		Default Value		
	Power On Sequence		88h		
	S/W Reset		88h		
	H/W Reset		88h		

STEP14S (B5h): STEP SET1

B5H	STEP14S (STEP SET 1)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX

STEP SET1	0	↑	1	-	1	0	1	1	0	1	0	1	(B5h)																	
1 st Parameter	1	↑	1	-	-	AVCLS.2-0			-	AVDDS.2-0			(45h)																	
Description	AVCLS[2:0]: AVCL Set.																													
	<table border="1"> <thead> <tr> <th>AVCLS [1:0]</th> <th>AVCL (V)</th> </tr> </thead> <tbody> <tr><td>00h</td><td>-3.08</td></tr> <tr><td>01h</td><td>-3.32</td></tr> <tr><td>02h</td><td>-3.59</td></tr> <tr><td>03h</td><td>-4.05</td></tr> <tr><td>04h</td><td>-4.40</td></tr> <tr><td>05h</td><td>-4.58</td></tr> <tr><td>06h</td><td>-4.78</td></tr> <tr><td>07h</td><td>-5.00</td></tr> </tbody> </table>						AVCLS [1:0]	AVCL (V)	00h	-3.08	01h	-3.32	02h	-3.59	03h	-4.05	04h	-4.40	05h	-4.58	06h	-4.78	07h	-5.00						
AVCLS [1:0]	AVCL (V)																													
00h	-3.08																													
01h	-3.32																													
02h	-3.59																													
03h	-4.05																													
04h	-4.40																													
05h	-4.58																													
06h	-4.78																													
07h	-5.00																													
Description	AVDDS[2:0]: AVDD Set.																													
	<table border="1"> <thead> <tr> <th>AVDDS[1:0]</th> <th>AVDD (V)</th> </tr> </thead> <tbody> <tr><td>00h</td><td>5.52</td></tr> <tr><td>01h</td><td>5.80</td></tr> <tr><td>02h</td><td>6.09</td></tr> <tr><td>03h</td><td>6.25</td></tr> <tr><td>04h</td><td>6.42</td></tr> <tr><td>05h</td><td>6.60</td></tr> <tr><td>06h</td><td>6.79</td></tr> <tr><td>07h</td><td>6.99</td></tr> </tbody> </table>						AVDDS[1:0]	AVDD (V)	00h	5.52	01h	5.80	02h	6.09	03h	6.25	04h	6.42	05h	6.60	06h	6.79	07h	6.99						
AVDDS[1:0]	AVDD (V)																													
00h	5.52																													
01h	5.80																													
02h	6.09																													
03h	6.25																													
04h	6.42																													
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Status	Default Value																													
Power On Sequence	45h																													
S/W Reset	45h																													
H/W Reset	45h																													

STEP23S (B6h): STEP SET2

B6H	STEP23S (STEP SET 2)																							
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
STEP SET2	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)											
1 st Parameter	1	↑	1	-	VGLS.3-0				VGHS.3-0				(89h)											
Description	VGLS[3:0]: VGL Set.																							
	VGLS[3:0]		VGL (V)			VGLS[3:0]		VGL (V)																
	00h		-6.80			08h		-10.00																
	01h		-7.20			09h		-10.40																
	02h		-7.60			0Ah		-10.80																
	03h		-8.00			0Bh		-11.30																
	04h		-8.40			0Ch		-11.70																
	05h		-8.78			0Dh		-12.00																
	06h		-9.15			0Eh		-12.52																
	07h		-9.56			0Fh		-12.75																
	VGHS[3:0]: VGH/VGHS Set.																							
	VGHS[3:0]		VGH/VGHS (V)			VGHS[3:0]		VGH/VGHS (V)																
	00h		7.5			08h		13.5																
	01h		8.0			09h		14.0																
	02h		8.5			0Ah		14.5																
	03h		9.0			0Bh		15.0																
	04h		11.0			0Ch		15.5																
	05h		12.0			0Dh		16.0																
	06h		12.5			0Eh		16.5																
	07h		13.0			0Fh		17.0																
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	Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
	Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																							

Default	Status		Default Value	
	Power On Sequence		89h	
	S/W Reset		89h	
	H/W Reset		89h	

SBSTS (B7h): SVDD_SVCL_SET

B6H	SBSTS (SVDD_SVCL_SET)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SVDD_SVCL_SET	0	↑	1	-	1	0	1	1	0	1	1	1	(B7h)
1 st Parameter	1	↑	1	-	-	SELN.2-0			-	-	SELP.1-0		(62h)

Description	SELN[2:0]: SVCL Set.												
	SELN[2:0]						SVCL (V)						
	00h						-3.346						
	01h						-3.500						
	02h						-3.663						
	03h						-3.835						
	04h						-4.220						
	05h						-4.400						
	06h						-4.588						
	07h						-4.788						
SELP[1:0]: SVDD Set.													
SELP[1:0]						SVDD (V)							
00h						6.243							
01h						6.420							
02h						6.600							
03h						6.794							
'-': Don't care													

Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						

		Sleep In	Yes								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>62h</td> </tr> <tr> <td>S/W Reset</td> <td>62h</td> </tr> <tr> <td>H/W Reset</td> <td>62h</td> </tr> </tbody> </table>			Status	Default Value	Power On Sequence	62h	S/W Reset	62h	H/W Reset	62h
	Status	Default Value									
	Power On Sequence	62h									
	S/W Reset	62h									
H/W Reset	62h										

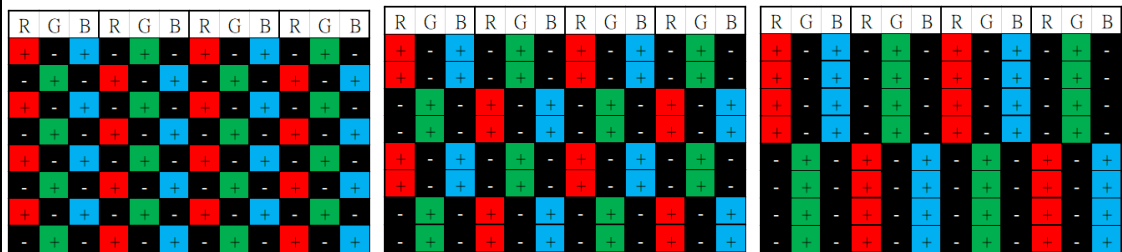
TCONS (BAh): TCON_SET

BAH	TCONS (TCON_SET)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TCON_SET	0	↑	1	-	1	0	1	1	1	0	1	0	(BAh)
1 st Parameter	1	↑	1	-	-	GATE_TUNE.2-0			-	-	NLINE.1-0		(00h)

NLINE[1:0]: dot inversion select

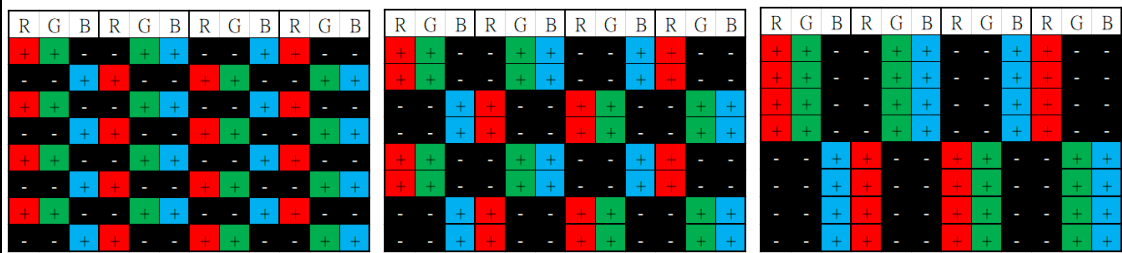
NLINE[1:0]	Dot Inversion Select
00h	1 line
01h	2 line
02h	4 line

-Single Gate: (when DUAL_EN = 0 in command D0h)



Description

-Dual Gate: (when DUAL_EN = 1 in command D0h)



'-': Don't care

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	Status		Default Value	
	Power On Sequence		00h	
	S/W Reset		00h	
	H/W Reset		00h	

RGBVBP (BBh): RGB_VBP

BBH	RGBVBP (RGB_VBP)																								
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RGB_VBP	0	↑	1	-	1	0	1	1	1	0	1	1	(BBh)												
1 st Parameter	1	↑	1	-	-	VBP.6-0						(08h)													
Description	VBP[6:0]: RGB interface Vsync back porch setting. '-': Don't care																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	08h																								
S/W Reset	08h																								
H/W Reset	08h																								

RGBHBP (BCh): RGB_HBP

BCBH	RGBHBP (RGB_HBP)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGB_HBP	0	↑	1	-	1	0	1	1	1	0	1	1	(BCh)
1 st Parameter	1	↑	1	-	-	HBP.6-0						(08h)	
Description	HBP[6:0]: RGB interface Hsync back porch setting. '-': Don't care												
Register Availability													

		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>08h</td> </tr> <tr> <td>S/W Reset</td> <td>08h</td> </tr> <tr> <td>H/W Reset</td> <td>08h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	08h	S/W Reset	08h	H/W Reset	08h				
Status	Default Value													
Power On Sequence	08h													
S/W Reset	08h													
H/W Reset	08h													

RGBSET (BDh): RGB_SET

BDH	RGBSET (RGB_SET)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGB_SET	0	↑	1	-	1	0	1	1	1	0	1	1	(BDh)
1 st Parameter	1	↑	1	-	WO	-	-	RCM	RGB_VDPO_L_XO_R	RGB_HDPO_L_XO_R	RGB_DEPO_L_XO_R	RGB_DCLK_POL_XOR	(00h)
Description	WO: Direct RGB mode.												
	WO		Mode										
	0		Memory										
	1		Shift register										
Description	RCM: RGB I/F enable mode selection.												
	RCM		Mode										
	0		RGB DE mode										
	1		RGB HV mode										
<p>RGB_VDPOL_XOR : Sets the signal polarity of the VSYNC pin. VSPL="0", Low active VSPL="1", High active</p> <p>RGB_HDPOL_XOR : Sets the signal polarity of the HSYNC pin. HSPL="0", Low active HSPL="1", High active</p> <p>RGB_DCLKPOL_XOR : Sets the signal polarity of the DOTCLK pin.</p>													

	<p>DPL = "0" The data is input on the positive edge of DOTCLK DPL = "1" The data is input on the negative edge of DOTCLK RGB_DEPOL_XOR : Sets the signal polarity of the ENABLE pin. EPL = "0" The data DB.7-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0". EPL = "1" The data DB.7-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1".</p> <p>'-': Don't care</p>												
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

CABCSET1 (BEH): CABC_SET1

BEH	CABCSET1 (CABC_SET1)												HEX
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	
CABC_SET1	0	↑	1	-	1	0	1	1	1	1	1	0	(BEh)
1 st Parameter	1	↑	1	-	-	-	-	LED_ PWM_ OEX	-	DSPO FFPW M_MD	PWM_ FIXON	PWM_ POLA R	(00h)
Description	<p>LED_PWM_OEX: LEDPWM Signal. "0": Output to CABCPWMP. "1": CABCPWMP is Floating.</p> <p>DSPOFFPWM_MD: initial state control of LEDPWM. "0": The initial state of LEDPWM is low. "1": The initial state of LEDPWM is high.</p> <p>PWM_FIXON: LEDPWM fix control. "0": LEDPWM control by CABC.</p>												

	<p>“1”: fix LEDPWM in “ON” status.</p> <p>PWM_POLAR: LEDPWM polarity control.</p> <p>“0”: polarity high.</p> <p>“1”: polarity low.</p> <p>‘-’: Don’t care</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												

CABCSET2 (BFh): CABC_SET2

BFH	CABCSET2 (CABC_SET2)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CABC_SET2	0	↑	1	-	1	0	1	1	1	1	1	1	(BFh)
1 st Parameter	1	↑	1	-	-	PWM_ SEGM ENT[2]	PWM_ SEGM ENT[1]	PWM_ SEGM ENT[0]	-	PWM_ CLK_ SEL[2]	PWM_ CLK_ SEL[1]	PWM_ CLK_ SEL[0]	(07h)
Description	PWM_SEGMENT[2:0] / PWM_CLK_SEL[2:0]:												
			PWM_SEGMENT[2:0]		00h	01h	02h	03h	04h	05h			
			PWM_CLK_SEL[2:0]										
			00h		39.2	78.7	158.7	322.6	666.7	1428.6			
			01h		19.6	39.4	79.4	161.3	333.3	714.3			
			02h		9.8	19.7	39.7	80.6	166.7	357.1			
			03h		4.9	9.8	19.8	40.3	83.3	178.6			
			04h		2.45	4.9	9.9	20.2	41.7	89.3			
			05h		1.23	2.5	5	10.1	20.8	44.6			
		06h		0.61	1.23	2.48	5	10.4	22.3				
		07h		0.31	0.62	1.24	2.5	5.2	11.2				

	Unit: kHz												
	‘-’: Don’t care												
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Status	Default Value												
Power On Sequence	07h												
S/W Reset	07h												
H/W Reset	07h												

FRCTRA1 (C0h): Frame Rate Control A1 in Normal Mode

C0H	FRCTRA1 (Frame Rate Control A1 in Normal Mode)												HEX												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
FRCTRA1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)												
1 st Parameter	1	↑	1	-	NLA	-	-	BPFPA.12-8					(80h)												
Description	<p>NLA : Inversion selection in normal mode. 0 : column inversion. 1 : dot inversion.</p> <p>BPFPA[12:0]: Back porch and Front porch setting in normal mode. The minimum setting is 0x04.</p> <p>‘-’: Don’t care</p>																								
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

Default	Status		Default Value	
	Power On Sequence		80h	
	S/W Reset		80h	
	H/W Reset		80h	

FRCTRA2 (C1h): Frame Rate Control A2 in Normal Mode

C1H	FRCTRA2 (Frame Rate Control A2 in Normal Mode)																								
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
FRCTRA2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)												
1 st Parameter	1	↑	1	-	BPFPA.7-0							(20h)													
Description	BPFPA[12:0]: Back porch and Front porch setting in normal mode. The minimum setting is 0x04. '-': Don't care																								
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Status	Default Value																								
Power On Sequence	20h																								
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H/W Reset	20h																								

FRCTRA3 (C2h): Frame Rate Control A3 in Normal Mode

C2H	FRCTRA3 (Frame Rate Control A3 in Normal Mode)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRCTRA3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)

1 st Parameter	1	↑	1	-	RTNA.7-0			(30h)
Description	RTNA[7:0]: Frame rate control in normal mode.							
	RTNA[7:0]	FR (Hz)	RTNA[7:0]	FR (Hz)	RTNA[7:0]	FR (Hz)	RTNA[7:0]	FR (Hz)
	00h	-	40h	46.28	80h	23.14	C0h	15.43
	01h	-	41h	45.57	81h	22.96	C1h	15.35
	02h	-	42h	44.88	82h	22.79	C2h	15.27
	03h	-	43h	44.21	83h	22.61	C3h	15.19
	04h	-	44h	43.56	84h	22.44	C4h	15.11
	05h	-	45h	42.93	85h	22.27	C5h	15.04
	06h	-	46h	42.32	86h	22.11	C6h	14.96
	07h	-	47h	41.72	87h	21.94	C7h	14.88
	08h	-	48h	41.14	88h	21.78	C8h	14.81
	09h	-	49h	40.58	89h	21.62	C9h	14.74
	0Ah	-	4Ah	40.03	8Ah	21.46	CAh	14.66
	0Bh	-	4Bh	39.49	8Bh	21.31	CBh	14.59
	0Ch	-	4Ch	38.97	8Ch	21.16	CCh	14.52
	0Dh	-	4Dh	38.47	8Dh	21.01	CDh	14.45
	0Eh	-	4Eh	37.98	8Eh	20.86	CEh	14.38
	0Fh	-	4Fh	37.49	8Fh	20.71	CFh	14.31
	10h	-	50h	37.03	90h	20.57	D0h	14.24
	11h	-	51h	36.57	91h	20.43	D1h	14.17
	12h	-	52h	36.12	92h	20.29	D2h	14.11
	13h	-	53h	35.69	93h	20.15	D3h	14.04
	14h	-	54h	35.26	94h	20.01	D4h	13.97
	15h	-	55h	34.85	95h	19.88	D5h	13.91
	16h	-	56h	34.44	96h	19.75	D6h	13.84
	17h	-	57h	34.05	97h	19.62	D7h	13.78
	18h	-	58h	33.66	98h	19.49	D8h	13.71
	19h	-	59h	33.28	99h	19.36	D9h	13.65
	1Ah	-	5Ah	32.91	9Ah	19.23	DAh	13.59
	1Bh	-	5Bh	32.55	9Bh	19.11	DBh	13.53
1Ch	-	5Ch	32.20	9Ch	18.99	DCh	13.46	
1Dh	-	5Dh	31.85	9Dh	18.87	DDh	13.40	
1Eh	-	5Eh	31.51	9Eh	18.75	DEh	13.34	
1Fh	-	5Fh	31.18	9Fh	18.63	DFh	13.28	
20h	-	60h	30.86	A0h	18.51	E0h	13.22	
21h	-	61h	30.54	A1h	18.40	E1h	13.16	

22h	-	62h	30.23	A2h	18.28	E2h	13.11
23h	-	63h	29.92	A3h	18.17	E3h	13.05
24h	-	64h	29.62	A4h	18.06	E4h	12.99
25h	-	65h	29.33	A5h	17.95	E5h	12.93
26h	-	66h	29.04	A6h	17.84	E6h	12.88
27h	-	67h	28.76	A7h	17.74	E7h	12.82
28h	74.05	68h	28.48	A8h	17.63	E8h	12.77
29h	72.25	69h	28.21	A9h	17.53	E9h	12.71
2Ah	70.53	6Ah	27.94	AAh	17.42	EAh	12.66
2Bh	68.89	6Bh	27.68	ABh	17.32	EBh	12.60
2Ch	67.32	6Ch	27.43	ACH	17.22	ECh	12.55
2Dh	65.82	6Dh	27.18	ADh	17.12	EDh	12.50
2Eh	64.39	6Eh	26.93	Aeh	17.02	Eeh	12.45
2Fh	63.02	6Fh	26.69	Afh	16.93	Efh	12.39
30h	61.71	70h	26.45	B0h	16.83	F0h	12.34
31h	60.45	71h	26.21	B1h	16.73	F1h	12.29
32h	59.24	72h	25.98	B2h	16.64	F2h	12.24
33h	58.08	73h	25.76	B3h	16.55	F3h	12.19
34h	56.96	74h	25.54	B4h	16.46	F4h	12.14
35h	55.89	75h	25.32	B5h	16.37	F5h	12.09
36h	54.85	76h	25.10	B6h	16.28	F6h	12.04
37h	53.86	77h	24.89	B7h	16.19	F7h	11.99
38h	52.89	78h	24.68	B8h	16.10	F8h	11.94
39h	51.97	79h	24.48	B9h	16.01	F9h	11.90
3Ah	51.07	7Ah	24.28	BAh	15.93	FAh	11.85
3Bh	50.20	7Bh	24.08	BBh	15.84	FBh	11.80
3Ch	49.37	7Ch	23.89	BCh	15.76	FCh	11.75
3Dh	48.56	7Dh	23.70	BDh	15.67	FDh	11.71
3Eh	47.78	7Eh	23.51	BEh	15.59	FEh	11.66
3Fh	47.02	7Fh	23.32	BFh	15.51	FFh	11.62

Note:

1. Frame rate = $1000 / ((2 * Y_Res. + 2 * BPFPA[12:0]) * RTNA[7:0] * tcon_clk / 1000000)$.
2. BPFPA[12:0] are in command C0h · C1h
3. In this frame rate table, Y_Res. = 390 · BPFPA[12:0] = 20h · tcon_clk = 400
4. The deviation of frame rate is +/- 5%.

	‘?’: Don't care												
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Status	Default Value												
Power On Sequence	30h												
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H/W Reset	30h												

FRCTRB1 (C3h): Frame Rate Control B1 in Idle Mode

C3H	FRCTRB1 (Frame Rate Control B1 in Idle Mode)												HEX												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
FRCTRB1	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)												
1 st Parameter	1	↑	1	-	NLB	-	-	BFPFB.12-8					(00h)												
Description	<p>NLB : Inversion selection in idle mode. 0 : column inversion. 1 : dot inversion.</p> <p>BFPFB[12:0]: Back porch and Front porch setting in idle mode. The minimum setting is 0x04.</p> <p>‘?’: Don't care</p>																								
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

Default	Status		Default Value	
	Power On Sequence		00h	
	S/W Reset		00h	
	H/W Reset		00h	

FRCTRB2 (C4h): Frame Rate Control B2 in Idle Mode

C4H	FRCTRB2 (Frame Rate Control B2 in Idle Mode)																								
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
FRCTRB2	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)												
1 st Parameter	1	↑	1	-	BFPB.7-0							(21h)													
Description	<p>BFPB[12:0]: Back porch and Front porch setting in idle mode. The minimum setting is 0x04.</p> <p>'-': Don't care</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Status	Default Value																								
Power On Sequence	21h																								
S/W Reset	21h																								
H/W Reset	21h																								

FRCTRB3 (C5h): Frame Rate Control B3 in Idle Mode

C5H	FRCTRB3 (Frame Rate Control B3 in Idle Mode)													
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
FRCTRB3	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)	
1 st Parameter	1	↑	1	-	RTNB.7-0								(31h)	
Description	RTNB[7:0]: Frame rate control in idle mode.													
	RTNB[7:0]	FR (Hz)	RTNB[7:0]	FR (Hz)	RTNB[7:0]	FR (Hz)	RTNB[7:0]	FR (Hz)	RTNB[7:0]	FR (Hz)	RTNB[7:0]	FR (Hz)	RTNB[7:0]	FR (Hz)
	00h	-	40h	46.28	80h	23.14	C0h	15.43						
	01h	-	41h	45.57	81h	22.96	C1h	15.35						
	02h	-	42h	44.88	82h	22.79	C2h	15.27						
	03h	-	43h	44.21	83h	22.61	C3h	15.19						
	04h	-	44h	43.56	84h	22.44	C4h	15.11						
	05h	-	45h	42.93	85h	22.27	C5h	15.04						
	06h	-	46h	42.32	86h	22.11	C6h	14.96						
	07h	-	47h	41.72	87h	21.94	C7h	14.88						
	08h	-	48h	41.14	88h	21.78	C8h	14.81						
	09h	-	49h	40.58	89h	21.62	C9h	14.74						
	0Ah	-	4Ah	40.03	8Ah	21.46	CAh	14.66						
	0Bh	-	4Bh	39.49	8Bh	21.31	CBh	14.59						
	0Ch	-	4Ch	38.97	8Ch	21.16	CCh	14.52						
	0Dh	-	4Dh	38.47	8Dh	21.01	CDh	14.45						
	0Eh	-	4Eh	37.98	8Eh	20.86	CEh	14.38						
	0Fh	-	4Fh	37.49	8Fh	20.71	CFh	14.31						
	10h	-	50h	37.03	90h	20.57	D0h	14.24						
	11h	-	51h	36.57	91h	20.43	D1h	14.17						
	12h	-	52h	36.12	92h	20.29	D2h	14.11						
	13h	-	53h	35.69	93h	20.15	D3h	14.04						
	14h	-	54h	35.26	94h	20.01	D4h	13.97						
	15h	-	55h	34.85	95h	19.88	D5h	13.91						
	16h	-	56h	34.44	96h	19.75	D6h	13.84						
	17h	-	57h	34.05	97h	19.62	D7h	13.78						
	18h	-	58h	33.66	98h	19.49	D8h	13.71						
	19h	-	59h	33.28	99h	19.36	D9h	13.65						
	1Ah	-	5Ah	32.91	9Ah	19.23	DAh	13.59						
	1Bh	-	5Bh	32.55	9Bh	19.11	DBh	13.53						
1Ch	-	5Ch	32.20	9Ch	18.99	DCh	13.46							
1Dh	-	5Dh	31.85	9Dh	18.87	DDh	13.40							

1Eh	-	5Eh	31.51	9Eh	18.75	DEh	13.34
1Fh	-	5Fh	31.18	9Fh	18.63	DFh	13.28
20h	-	60h	30.86	A0h	18.51	E0h	13.22
21h	-	61h	30.54	A1h	18.40	E1h	13.16
22h	-	62h	30.23	A2h	18.28	E2h	13.11
23h	-	63h	29.92	A3h	18.17	E3h	13.05
24h	-	64h	29.62	A4h	18.06	E4h	12.99
25h	-	65h	29.33	A5h	17.95	E5h	12.93
26h	-	66h	29.04	A6h	17.84	E6h	12.88
27h	-	67h	28.76	A7h	17.74	E7h	12.82
28h	74.05	68h	28.48	A8h	17.63	E8h	12.77
29h	72.25	69h	28.21	A9h	17.53	E9h	12.71
2Ah	70.53	6Ah	27.94	AAh	17.42	EAh	12.66
2Bh	68.89	6Bh	27.68	ABh	17.32	EBh	12.60
2Ch	67.32	6Ch	27.43	ACh	17.22	ECh	12.55
2Dh	65.82	6Dh	27.18	ADh	17.12	EDh	12.50
2Eh	64.39	6Eh	26.93	A Eh	17.02	EEh	12.45
2Fh	63.02	6Fh	26.69	AFh	16.93	EFh	12.39
30h	61.71	70h	26.45	B0h	16.83	F0h	12.34
31h	60.45	71h	26.21	B1h	16.73	F1h	12.29
32h	59.24	72h	25.98	B2h	16.64	F2h	12.24
33h	58.08	73h	25.76	B3h	16.55	F3h	12.19
34h	56.96	74h	25.54	B4h	16.46	F4h	12.14
35h	55.89	75h	25.32	B5h	16.37	F5h	12.09
36h	54.85	76h	25.10	B6h	16.28	F6h	12.04
37h	53.86	77h	24.89	B7h	16.19	F7h	11.99
38h	52.89	78h	24.68	B8h	16.10	F8h	11.94
39h	51.97	79h	24.48	B9h	16.01	F9h	11.90
3Ah	51.07	7Ah	24.28	BAh	15.93	FAh	11.85
3Bh	50.20	7Bh	24.08	BBh	15.84	FBh	11.80
3Ch	49.37	7Ch	23.89	BCh	15.76	FCh	11.75
3Dh	48.56	7Dh	23.70	BDh	15.67	FDh	11.71
3Eh	47.78	7Eh	23.51	BEh	15.59	FEh	11.66
3Fh	47.02	7Fh	23.32	BFh	15.51	FFh	11.62

Note:

1. Frame rate = $1000 / ((2 * Y_Res. + 2 * BPFPA[12:0]) * RTNA[7:0] * tcon_clk / 1000000)$.

	<p>2. BPFPA[12:0] are in command C0h · C1h</p> <p>3. In this frame rate table, Y_Res. = 390 · BPFPA[12:0] = 20h · tcon_clk = 400</p> <p>4. The deviation of frame rate is +/- 5%.</p> <p>'-': Don't care</p>												
Register Availability	<table border="1" data-bbox="405 443 1362 748"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value												
Power On Sequence	31h												
S/W Reset	31h												
H/W Reset	31h												

PWRCTRA1 (C6h): Power Control A1 in Normal Mode

C6H	PWRCTRA1 (Power Control A1 in Normal Mode)															
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX			
PWRCTRA1	0	↑	1	-	1	1	0	0	0	1	1	0	(C6h)			
1 st Parameter	1	↑	1	-	DCA3.1-0		DCA2S.1-0		DCA2.1-0		DCA1.1-0		(A9h)			
Description	DCA3[1:0]: STP3(VGL) booster clock selection in normal mode.															
	DCA3[1:0]				CK_STP3 (MHz)											
	00h				9											
	01h				6.67 (from osc1)											
	02h				5 (from osc1)											
	03h				4.5											
	DCA2S[1:0]: STP2S(VGHS) booster clock selection in normal mode.															
	DCA2S[1:0]				CK_STP2S (MHz)											
	00h				6.67 (from osc1)											
	01h				6											
	02h				5 (from osc1)											
	03h				4.5											
	DCA2[1:0]: STP2(VGH) booster clock selection in normal mode.															
	DCA2[1:0]				CK_STP2 (MHz)											
	00h				6.67 (from osc1)											
	01h				6											
	02h				5 (from osc1)											
	03h				4.5											
	DCA1[1:0]: STP1(AVDD) booster clock selection in normal mode.															
	DCA1[1:0]				CK_STP1 (MHz)											
00h				18												
01h				13 (from osc1)												
02h				10 (from osc1)												
03h				5 (from osc1)												
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Register Availability	<table border="1"> <thead> <tr> <th>Status</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> </tr> </tbody> </table>						Status	Normal Mode On, Idle Mode Off, Sleep Out	<table border="1"> <thead> <tr> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Yes</td> </tr> </tbody> </table>						Availability	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes								
Partial Mode On, Idle Mode Off, Sleep Out	Yes								
Partial Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
Default	<table border="1"> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <td>Power On Sequence</td> <td>A9h</td> </tr> <tr> <td>S/W Reset</td> <td>A9h</td> </tr> <tr> <td>H/W Reset</td> <td>A9h</td> </tr> </table>	Status	Default Value	Power On Sequence	A9h	S/W Reset	A9h	H/W Reset	A9h
Status	Default Value								
Power On Sequence	A9h								
S/W Reset	A9h								
H/W Reset	A9h								

PWRCTRA2 (C7h): Power Control A2 in Normal Mode

C7H	PWRCTRA2 (Power Control A2 in Normal Mode)																														
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
PWRCTRA2	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)																		
1 st Parameter	1	↑	1	-	-	APA.2-0			SAPA.1-0		DCA4.1-0		(41h)																		
Description	APA[2:0]: Adjust OPAMP input differential-pair bias current in normal mode.																														
	<table border="1"> <thead> <tr> <th>APA[2:0]</th> <th></th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Stops</td> </tr> <tr> <td>01h</td> <td>1.0x</td> </tr> <tr> <td>02h</td> <td>1.5x</td> </tr> <tr> <td>03h</td> <td>2.0x</td> </tr> <tr> <td>04h</td> <td>2.5x</td> </tr> <tr> <td>05h</td> <td>3.0x</td> </tr> <tr> <td>06h</td> <td>3.5x</td> </tr> <tr> <td>07h</td> <td>4.0x</td> </tr> </tbody> </table>													APA[2:0]		00h	Stops	01h	1.0x	02h	1.5x	03h	2.0x	04h	2.5x	05h	3.0x	06h	3.5x	07h	4.0x
	APA[2:0]																														
	00h	Stops																													
	01h	1.0x																													
	02h	1.5x																													
	03h	2.0x																													
	04h	2.5x																													
	05h	3.0x																													
	06h	3.5x																													
	07h	4.0x																													
	SAPA[1:0]: Adjust OPAMP output mos bias current in normal mode.																														
	<table border="1"> <thead> <tr> <th>SAPA[1:0]</th> <th></th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>0.1x</td> </tr> <tr> <td>01h</td> <td>0.2x</td> </tr> <tr> <td>02h</td> <td>0.3x</td> </tr> <tr> <td>03h</td> <td>0.4x</td> </tr> </tbody> </table>													SAPA[1:0]		00h	0.1x	01h	0.2x	02h	0.3x	03h	0.4x								
	SAPA[1:0]																														
	00h	0.1x																													
	01h	0.2x																													
	02h	0.3x																													
	03h	0.4x																													
	DCA4[1:0]: STP4(AVCL) booster clock selection in normal mode.																														
	<table border="1"> <thead> <tr> <th>DCA4[1:0]</th> <th>CK_STP4 (MHz)</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>18</td> </tr> </tbody> </table>													DCA4[1:0]	CK_STP4 (MHz)	00h	18														
	DCA4[1:0]	CK_STP4 (MHz)																													
	00h	18																													

	01h	13 (from osc1)												
	02h	10 (from osc1)												
	03h	5 (from osc1)												
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Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode Off, Sleep Out	Yes													
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>41h</td> </tr> <tr> <td>S/W Reset</td> <td>41h</td> </tr> <tr> <td>H/W Reset</td> <td>41h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	41h	S/W Reset	41h	H/W Reset	41h				
Status	Default Value													
Power On Sequence	41h													
S/W Reset	41h													
H/W Reset	41h													

PWRCTRA3 (C8h): Power Control A3 in Normal Mode

C8H	PWRCTRA3 (Power Control A3 in Normal Mode)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCTRA3	0	↑	1	-	1	1	0	0	1	0	0	0	(C8h)
1 st Parameter	1	↑	1	-	CLK_SNA.1-0		CLK_SPA.1-0		-	-	CLK_HYA.1-0		(51h)
Description	CLK_SNA[1:0]: Source(SVCL) booster clock selection in normal mode.												
	CLK_SNA[1:0]		CLKN										
	00h		10 (from osc1)										
	01h		9										
	02h		6.67 (from osc1)										
	03h		6										
	CLK_SPA[1:0]: Source(SVDD) booster clock selection in normal mode.												
	CLK_SPA[1:0]		CLKP										
	00h		10 (from osc1)										
	01h		9										
	02h		6.67 (from osc1)										
	03h		6										

	<p>CLK_HYA[1:0]:</p> <table border="1"> <thead> <tr> <th>CLK_HYA[1:0]</th> <th>CLKHY</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>10 (from osc1)</td> </tr> <tr> <td>01h</td> <td>9</td> </tr> <tr> <td>02h</td> <td>6.67 (from osc1)</td> </tr> <tr> <td>03h</td> <td>6</td> </tr> </tbody> </table> <p>'-': Don't care</p>	CLK_HYA[1:0]	CLKHY	00h	10 (from osc1)	01h	9	02h	6.67 (from osc1)	03h	6		
CLK_HYA[1:0]	CLKHY												
00h	10 (from osc1)												
01h	9												
02h	6.67 (from osc1)												
03h	6												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>51h</td> </tr> <tr> <td>S/W Reset</td> <td>51h</td> </tr> <tr> <td>H/W Reset</td> <td>51h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	51h	S/W Reset	51h	H/W Reset	51h				
Status	Default Value												
Power On Sequence	51h												
S/W Reset	51h												
H/W Reset	51h												

PWRCTRB1 (C9h): Power Control B1 in Idle Mode

C9H	PWRCTRB1 (Power Control B1 in Idle Mode)												HEX
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCTRB1	0	↑	1	-	1	1	0	0	1	0	0	1	(C9h)
1 st Parameter	1	↑	1	-	DCB3.1-0		DCB2S.1-0		DCB2.1-0		DCB1.1-0		(A9h)
Description	DCB3[1:0]: STP3(VGL) booster clock selection in idle mode.												
	DCB3[1:0]		CK_STP3 (MHz)										
	00h		9										
	01h		6.67 (from osc1)										
	02h		5 (from osc1)										
03h		4.5											
DCB2S[1:0]: STP2S(VGHS) booster clock selection in idle mode.													
DCB2S[1:0]		CK_STP2S (MHz)											

	00h	6.67 (from osc1)												
	01h	6												
	02h	5 (from osc1)												
	03h	4.5												
DCB2[1:0]: STP2(VGH) booster clock selection in idle mode.														
	DCB2[1:0]	CK_STP2 (MHz)												
	00h	6.67 (from osc1)												
	01h	6												
	02h	5 (from osc1)												
	03h	4.5												
DCB1[1:0]: STP1(AVDD) booster clock selection in idle mode.														
	DCB1[1:0]	CK_STP1 (MHz)												
	00h	18												
	01h	13 (from osc1)												
	02h	10 (from osc1)												
	03h	5 (from osc1)												
'-': Don't care														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value													
Power On Sequence	A9h													
S/W Reset	A9h													
H/W Reset	A9h													

PWRCTRB2 (CAh): Power Control B2 in Idle Mode

CAH	PWRCTRB2 (Power Control B2 in Idle Mode)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCTRB2	0	↑	1	-	1	1	0	0	1	0	1	0	(CAh)

1 st Parameter	1	↑	1	-	-	APB.2-0	SAPB.1-0	DCB4.1-0	(41h)												
Description	APB[2:0]: Adjust OPAMP input differential-pair bias current in idle mode.																				
	APB[2:0]																				
	00h Stops																				
	01h 1.0x																				
	02h 1.5x																				
	03h 2.0x																				
	04h 2.5x																				
	05h 3.0x																				
	06h 3.5x																				
	07h 4.0x																				
	SAPB[1:0]: Adjust OPAMP output mos bias current in idle mode.																				
	SAPB[1:0]																				
	00h 0.1x																				
	01h 0.2x																				
	02h 0.3x																				
03h 0.4x																					
DCB4[1:0]: STP4(AVCL) booster clock selection in idle mode.																					
DCB4[1:0] CK_STP4 (MHz)																					
00h 18																					
01h 13 (from osc1)																					
02h 10 (from osc1)																					
03h 5 (from osc1)																					
'-': Don't care																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>									Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode On, Sleep Out	Yes																				
Sleep In	Yes																				

Default	Status	Default Value
	Power On Sequence	41h
	S/W Reset	41h
	H/W Reset	41h

PWRCTRB3 (CBh): Power Control B3 in Idle Mode

CBH	PWRCTRB3 (Power Control B3 in Idle Mode)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCTRB3	0	↑	1	-	1	1	0	0	1	0	1	1	(CBh)
1 st Parameter	1	↑	1	-	CLK_SNB.1-0		CLK_SPB.1-0		-	-	CLK_HYB.1-0		(51h)
Description	CLK_SNB[1:0]: Source(SVCL) booster clock selection in idle mode.												
	CLK_SNB[1:0]		CLKN										
	00h		10 (from osc1)										
	01h		9										
	02h		6.67 (from osc1)										
	03h		6										
	CLK_SPB[1:0]: Source(SVDD) booster clock selection in idle mode.												
	CLK_SPB[1:0]		CLKP										
	00h		10 (from osc1)										
	01h		9										
	02h		6.67 (from osc1)										
	03h		6										
	CLK_HYB[1:0]:												
	CLK_HYB[1:0]		CLKHY										
	00h		9										
	01h		6.67 (from osc1)										
	02h		6										
03h		4.5 (from osc1)											
'-': Don't care													
Register Availability													

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Status	Default Value													
Power On Sequence	51h													
S/W Reset	51h													
H/W Reset	51h													

DSTBDSL (CFh): DSTB_DSLP

CFH	DSTBDSL (DSTB_DSLP)																								
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
DSTBDSL	0	↑	1	-	1	1	0	0	1	0	1	1	(CFh)												
1 st Parameter	1	↑	1	-	-	-	-	-	-	-	DSTB _EN	DSL P _EN	(00h)												
Description	<p>DSTB_EN: "0": No Function. "1": Deep Standby mode.</p> <p>DSL_P_EN: "0": Sleep In mode. "1": Deep Sleep In mode.</p> <p><i>Note1: It will be necessary to stay at sleep in mode before enter deep sleep in mode if P80 · SPI and QSPI is used.</i> <i>Note2: It will be necessary to stay at ULPS mode before enter deep sleep in mode if MIPI is used.</i> <i>Note3: No matter what status is, it is allowed to enter deep standby mode.</i> <i>Note4: It will be necessary to set HWRST or toggle CSX 7-8 times to leave deep standby mode.</i> <i>Note5: It will be necessary to set HWRST or set DSL_P_EN=0 to leave deep sleep in mode.</i> <i>Note6: It will be necessary to wait 10msec after set DSL_P_EN=0 to leave deep sleep in mode before sending the other commands.</i></p> <p>'-': Don't care</p>																								
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Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								

RESSET1 (D0h): Resolution Set 1

D0H	RESSET1 (Resolution Set 1)												HEX
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	
RESSET1	0	↑	1	-	1	1	0	1	0	0	0	0	(D0h)
1 st Parameter	1	↑	1	-	DUAL_E N	SSI	-	X_RE S.8	-	Y_RES.10-8			(91h)

DUAL_EN:
 "0": Single gate.
 "1": Dual gate.

Dual-Gate

Single-Gate

SSI:
 "0": Normal mode.
 "1": Partial off Source OP mode.

X_RES.8-0: Set X-Resolution(Source).
Y_RES.10-0: Set Y-Resolution(Gate).

*Note1: If DUAL_EN set 0 and Horizontal Scroll isn't applied,
 the X_RES must be a multiple of 4 pixel and no fewer than 92 pixel.*

*Note2: If DUAL_EN set 1 and Horizontal Scroll isn't applied,
 the X_RES must be a multiple of 8 Pixel and no fewer than 184 pixel.*

*Note3: If DUAL_EN set 0 and Horizontal Scroll is applied,
 the X_RES must be a multiple of 12 pixel and no fewer than 96 pixel.*

*Note4: If DUAL_EN set 1 and Horizontal Scroll is applied,
 the X_RES must be a multiple of 24 Pixel and no fewer than 192 pixel.*

	<p>Note5: The Y_RES must be more than or equal to 10 pixel.</p> <p>'-': Don't care</p>												
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Status	Default Value												
Power On Sequence	91h												
S/W Reset	91h												
H/W Reset	91h												

RESET2 (D1h): Resolution Set 2

D1H	RESET2 (Resolution Set 2)												HEX			
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX			
RESET2	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)			
1 st Parameter	1	↑	1	-	X_RES.7-0							(68h)				
Description	<p>X_RES.8-0: Set X-Resolution(Source).</p> <p>Note1: If DUAL_EN set 0 and Horizontal Scroll isn't applied, the X_RES must be a multiple of 4 pixel and no fewer than 92 pixel.</p> <p>Note2: If DUAL_EN set 1 and Horizontal Scroll isn't applied, the X_RES must be a multiple of 8 Pixel and no fewer than 184 pixel.</p> <p>Note3: If DUAL_EN set 0 and Horizontal Scroll is applied, the X_RES must be a multiple of 12 pixel and no fewer than 96 pixel.</p> <p>Note4: If DUAL_EN set 1 and Horizontal Scroll is applied, the X_RES must be a multiple of 24 Pixel and no fewer than 192 pixel.</p> <p>'-': Don't care</p>															
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Status	Availability															

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	Status	Default Value								
	Power On Sequence	68h								
	S/W Reset	68h								
H/W Reset	68h									

RESSET3 (D2h): Resolution Set 3

D2H	RESSET3 (Resolution Set 3)																								
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RESSET3	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)												
1 st Parameter	1	↑	1	-	Y_RES.7-0							(86h)													
Description	<p>Y_RES.8-0: Set Y-Resolution(Gate).</p> <p><i>Note1: The Y_RES must be more than or equal to 10.</i></p> <p>'-': Don't care</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	86h																								
S/W Reset	86h																								
H/W Reset	86h																								

VCMOFSET (DDh): VCOM OFFSET SET

DDH	VCMOFSET (VCOM OFFSET SET)
-----	----------------------------

Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
VCMOFSET	0	↑	1	-	1	1	0	1	1	1	0	1	(DDh)												
1 st Parameter	1	↑	1	-	-	VMF.6-0						(40h)													
Description	VMF[6:0]: VCOMS offset setting																								
		VMF[6]	VMF[5:0]	GVDD	GVCL	VSF	VCOM																		
		0	000000	VRHP-64d	VRHN+64d	VCM-64d	0																		
		0	000001	VRHP-63d	VRHN+63d	VCM-63d	0																		
		0	000010	VRHP-62d	VRHN+62d	VCM-62d	0																		
		0					0																		
		0	111110	VRHP-2d	VRHN+2d	VCM-2d	0																		
		0	111111	VRHP-1d	VRHN+1d	VCM-1d	0																		
		1	000000	VRHP	VRHN	VCM	0																		
		1	000001	VRHP+1d	VRHN-1d	VCM+1d	0																		
		1	000010	VRHP+2d	VRHN-2d	VCM+2d	0																		
		1					0																		
		1	111110	VRHP+62d	VRHN-62d	VCM+62d	0																		
	1	111111	VRHP+63d	VRHN-63d	VCM+63d	0																			
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	Status	Default Value																							
	Power On Sequence	40h																							
	S/W Reset	40h																							
H/W Reset	40h																								

VCMOFNSET (DEh): VCOM OFFSET NEW SET

DEH	VCMOFNSET (VCOM OFFSET NEW SET)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VCMOFNSET	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)

1 st Parameter	1	↑	1	-	-	VMF_NEW.6-0						(40h)												
Description	VMF_NEW[6:0]: VCOMS offset new setting																							
	VMF_NEW[6]	VMF_NEW[5:0]	GVDD	GVCL	VSF	VCOM																		
	0	000000	VRHP-64d	VRHN+64d	VCM-64d	0																		
	0	000001	VRHP-63d	VRHN+63d	VCM-63d	0																		
	0	000010	VRHP-62d	VRHN+62d	VCM-62d	0																		
	0					0																		
	0	111110	VRHP-2d	VRHN+2d	VCM-2d	0																		
	0	111111	VRHP-1d	VRHN+1d	VCM-1d	0																		
	1	000000	VRHP	VRHN	VCM	0																		
	1	000001	VRHP+1d	VRHN-1d	VCM+1d	0																		
	1	000010	VRHP+2d	VRHN-2d	VCM+2d	0																		
	1					0																		
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	Status	Default Value																						
	Power On Sequence	40h																						
	S/W Reset	40h																						
H/W Reset	40h																							

GAMCTRP1 (E0h): Positive Voltage Gamma Control

E0H	GAMCTRP1 (Positive Voltage Gamma Control)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMCTRP1	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1 st Parameter	1	↑	1	-	VC63P.3-0				VC0P.3-0				(F0h)
2 nd Parameter	1	↑	1	-	-	-	VC1P.5-0						(03h)

3 rd Parameter	1	↑	1	-	-	-	VC2P.5-0		(05h)		
4 th Parameter	1	↑	1	-	-	-	-	VC4P.4-0	(09h)		
5 th Parameter	1	↑	1	-	-	-	-	VC6P.4-0	(0Ch)		
6 th Parameter	1	↑	1	-	-	AJ0P.2-0		VC13P.3-0	(0Fh)		
7 th Parameter	1	↑	1	-	-	VC20P.6-0			(3Eh)		
8 th Parameter	1	↑	1	-	-	VC36P.2-0	-	VC27P.2-0	(77h)		
9 th Parameter	1	↑	1	-	-	VC43P.6-0			(4Fh)		
10 th Parameter	1	↑	1	-	-	AJ1P.2-0		VC50P.3-0	(0Fh)		
11 th Parameter	1	↑	1	-	-	-	-	VC57P.4-0	(17h)		
12 th Parameter	1	↑	1	-	-	-	-	VC59P.4-0	(17h)		
13 th Parameter	1	↑	1	-	-	-	VC61P.5-0		(21h)		
14 th Parameter	1	↑	1	-	-	-	VC62P.5-0		(23h)		
Description	Adjust the gamma characteristics of the TFT panel. Please refer to 9.6. Default value:										
	Register		Value(hex)								
	VC0P[3:0]		0								
	VC1P[5:0]		3								
	VC2P[5:0]		5								
	VC4P[4:0]		9								
	VC6P[4:0]		C								
	VC13P[3:0]		F								
	VC20P[6:0]		3E								
	VC27P[2:0]		7								
	VC36P[2:0]		7								
	VC43P[6:0]		4F								
	VC50P[3:0]		F								
	VC57P[4:0]		17								
	VC59P[4:0]		17								
	VC61P[5:0]		21								
	VC62P[5:0]		23								
	VC63P[3:0]		F								
	AJ0P[1:0]		0								
AJ1P[1:0]		0									
': Don't care											
Register Availability											

	Status		Availability	
	Normal Mode On, Idle Mode Off, Sleep Out		Yes	
	Normal Mode On, Idle Mode On, Sleep Out		Yes	
	Partial Mode On, Idle Mode Off, Sleep Out		Yes	
	Partial Mode On, Idle Mode On, Sleep Out		Yes	
	Sleep In		Yes	
Default	Status		Default Value	
	Power On Sequence		Refer to description	
	S/W Reset		Refer to description	
	H/W Reset		Refer to description	

GAMCTRN1 (E1h): Negative Voltage Gamma Control

E1H	GAMCTRN1 (Negative Voltage Gamma Control)												
Inst / Para	D/CX	WRX	RDX	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMCTRN1	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)
1 st Parameter	1	↑	1	-	VC63N.3-0				VC0N.3-0				(F0h)
2 nd Parameter	1	↑	1	-	-	-	VC1N.5-0						(03h)
3 rd Parameter	1	↑	1	-	-	-	VC2N.5-0						(05h)
4 th Parameter	1	↑	1	-	-	-	-	VC4N.4-0					(09h)
5 th Parameter	1	↑	1	-	-	-	-	VC6N.4-0					(0Ch)
6 th Parameter	1	↑	1	-	-	AJ0N.2-0			VC13N.3-0				(0Fh)
7 th Parameter	1	↑	1	-	-	VC20N.6-0							(3Eh)
8 th Parameter	1	↑	1	-	-	VC36N.2-0			-	VC27N.2-0			(77h)
9 th Parameter	1	↑	1	-	-	VC43N.6-0							(4Fh)
10 th Parameter	1	↑	1	-	-	AJ1N.2-0			VC50N.3-0				(0Fh)
11 th Parameter	1	↑	1	-	-	-	-	VC57N.4-0					(17h)
12 th Parameter	1	↑	1	-	-	-	-	VC59N.4-0					(17h)
13 th Parameter	1	↑	1	-	-	-	VC61N.5-0						(21h)
14 th Parameter	1	↑	1	-	-	-	VC62N.5-0						(23h)

Description	Adjust the gamma characteristics of the TFT panel. Please refer to 9.6. Default value:													
	Register	Value(hex)												
	VC0N[3:0]	0												
	VC1N[5:0]	3												
	VC2N[5:0]	5												
	VC4N[4:0]	9												
	VC6N[4:0]	C												
	VC13N[3:0]	F												
	VC20N[6:0]	3E												
	VC27N[2:0]	7												
	VC36N[2:0]	7												
	VC43N[6:0]	4F												
	VC50N[3:0]	F												
	VC57N[4:0]	17												
	VC59N[4:0]	17												
	VC61N[5:0]	21												
	VC62N[5:0]	23												
	VC63N[3:0]	F												
AJ0N[1:0]	0													
AJ1N[1:0]	0													
'-': Don't care														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Refer to description</td> </tr> <tr> <td>S/W Reset</td> <td>Refer to description</td> </tr> <tr> <td>H/W Reset</td> <td>Refer to description</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Refer to description	S/W Reset	Refer to description	H/W Reset	Refer to description				
Status	Default Value													
Power On Sequence	Refer to description													
S/W Reset	Refer to description													
H/W Reset	Refer to description													

14 REVISION HISTORY

Version	Date	Description
V0.0	2021/09	Preliminary
V0.1	2021/10	Preliminary
V0.2	2021/12	Preliminary
V0.3	2022/03	Preliminary
V1.0	2022/08	First Issue